

ZRS

REV : A01

- @ : Nopop Component
- 1@ : ZUMA Used Only
- 2@ : Riker Used Only
- 3@ : ZRS with discrete Used Only
- 4@ : ZUMA & Zanzibar Used Only
with BCM4401E w/o Docking and Smart card
- 5@ : Rikers & Suva Used Only
with BCM5752/Docking/Smart Card
- 6@ : Suva Used Only
- 7@ : Rikers/Zanzibar/ZUMA Used Only

Config. TABLE

Project	Config.
ZUMA	1@ + 4@ +7@
Zanzibar	3@ + 4@ + 7@
Suva	3@ + 5@ + 6@
Rikers	2@ + 3@ + 5@ + 7@

Yonah Schematics with Capture CIS and Function Field

uFCPGA Yonah

12/13/2005

REV : 2.0

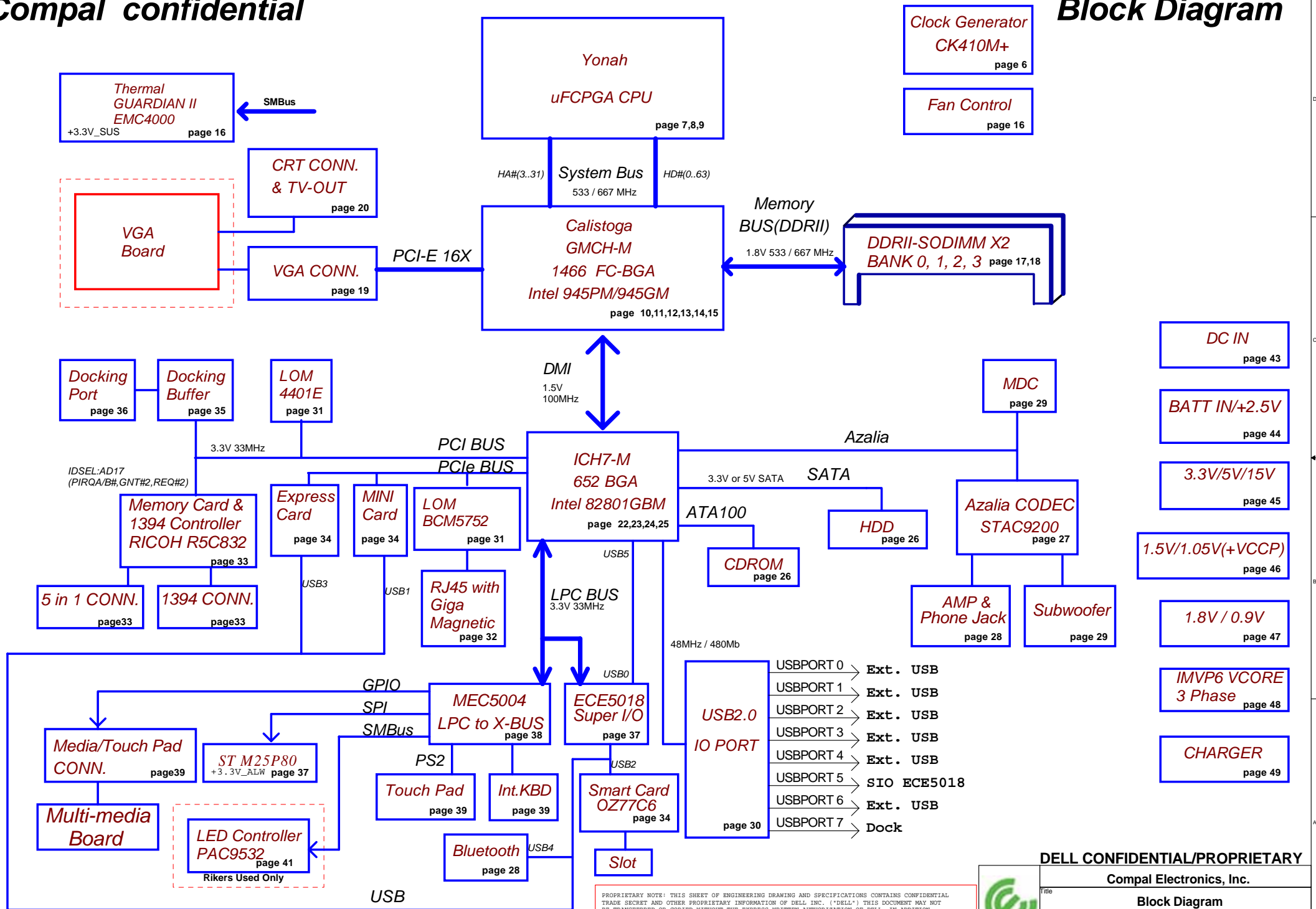
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Block Diagram

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PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_SRC	+15V_SUS +5V_SUS +3.3V_SUS +1.8V_SUS	+5V_RUN +3.3V_RUN +2.5V_RUN +1.8V_RUN +0.9V_DDR_VTT +VCC_CORE +1.05V_VCCP
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

	USB PORT#	Description
ICH7-M	0	SUPER I/O ECE5018
	1	JUSB_R (Ext Back Right Bottom)
	2	JUSB_S (Ext Side Bottom)
	3	JUSB_R (Ext Back Right Top)
	4	JUSB_L (Ext Back Left Top)
	5	JUSB_S (Ext Side Top)
	6	JUSB_L (Ext Back Left Bottom)
SIO ECE5018	7	DOCKING
	0	ICH7-M
	1	MINI CARD WLAN
	2	SMART CARD
	3	EXPRESS CARD
	4	BLUE TOOTH

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
LAN	AD16	REQ#3/GNT#3	IRQB
Dock	AD24	REQ#0/GNT#0	IRQA
R5C832	AD17	REQ#2/GNT#2	IRQC,D

PCI EXPRESS	DESTINATION
Lane 1	No
Lane 2	MINI CARD WLAN
Lane 3	GIGA LAN
Lane 4	EXPRESS CARD

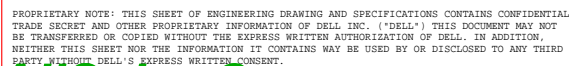
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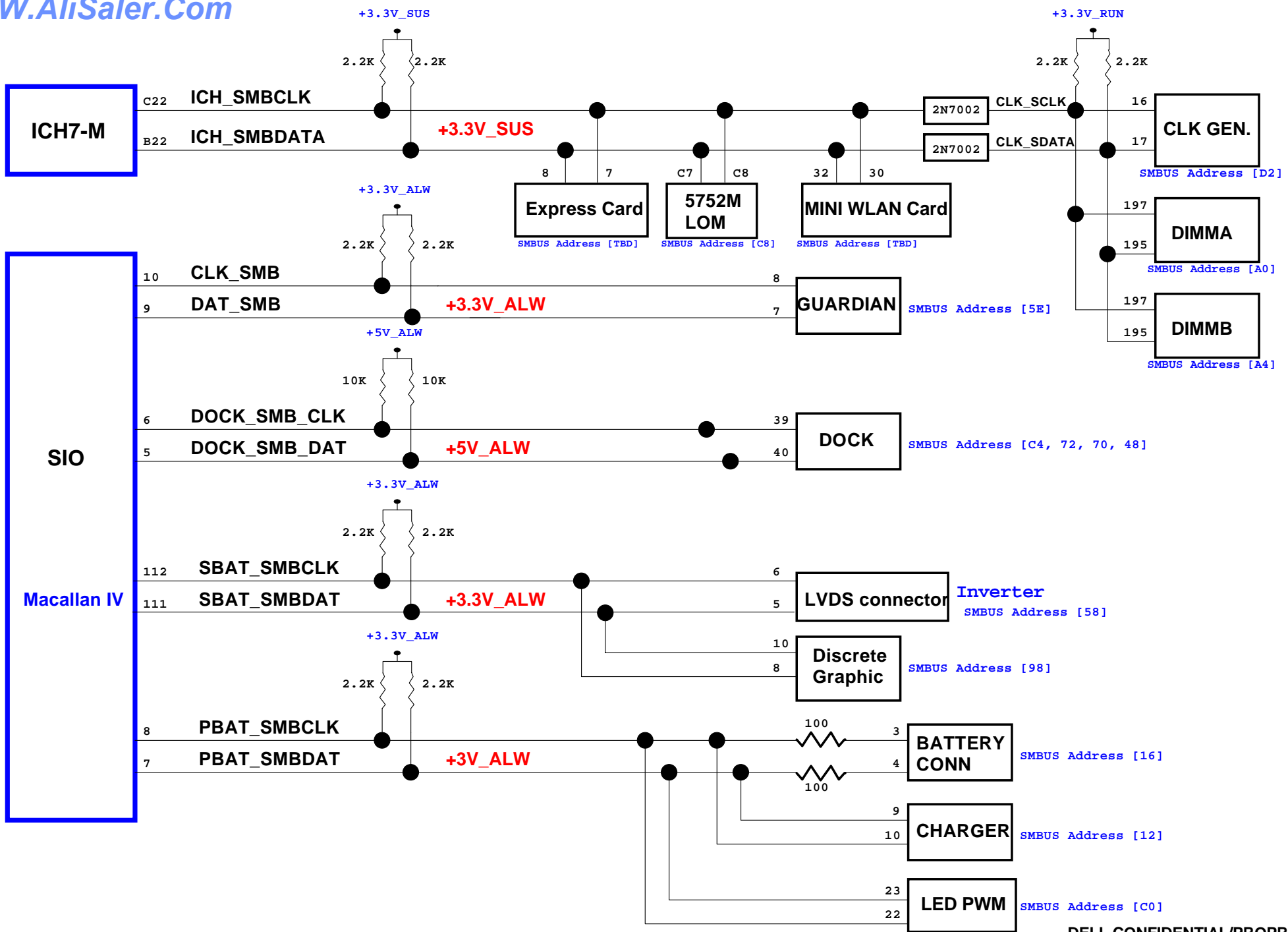


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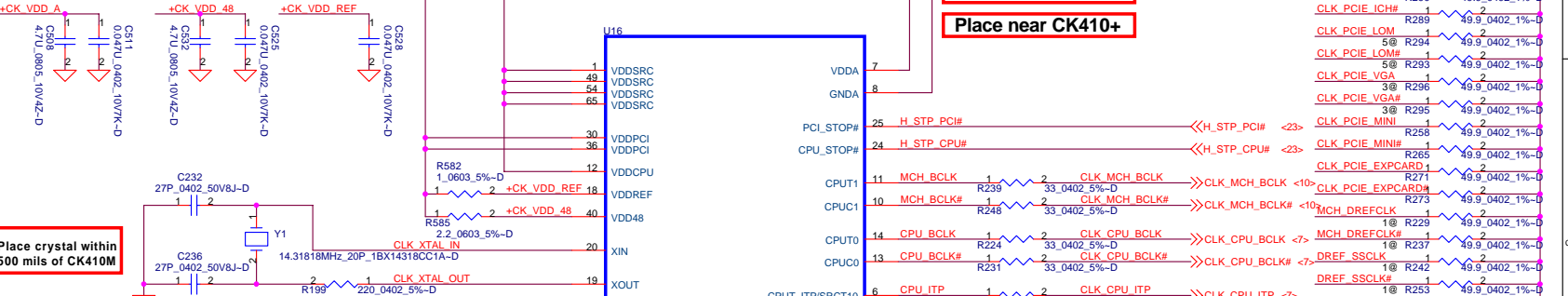
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SMBUS TOPOLOGY

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Timing diagram for the CPU_MCH_BSEL0 signal. The diagram shows the relationship between various signals and CPU_MCH_BSEL0 over time. Signals include CLK_ICH_48M, CLK_SMCARD_48M, CPU_MCH_BSEL0, CPU_MCH_BSEL1, CPU_MCH_BSEL2, CLK_PCI_5004, CLK_PCI_5018, CLK_PCI_LAN_LPC, CLK_PCI_PCCARD, CLK_PCI_DOCK, CLK_ICH_14M, CLK_SIO_14M, MCH_DREFCLK, MCH_DREFCLK#, MCH_DREFCLK#, CLK_PCI_ICH, CLK_PCI_ICH#, and +3.3V_RUN. The diagram is divided into two sections: the left section shows the initial setup and the right section shows the main operation. The left section shows the initial setup of the CPU_MCH_BSEL0 signal, which is initially high and then transitions to low. The right section shows the main operation of the CPU_MCH_BSEL0 signal, which is low and then transitions to high. The diagram includes a legend for the signals and a scale bar for time.

<48> CLK_ENABLE# >>> CLK_ENABLE# Vlt_PwrGnd#/PD

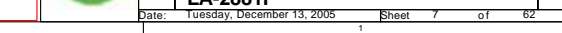
CLK_SCLK 16 SMCLK SRCT4 58 PCIE_L0M 1 2 CLK_PCIE_L0M 2 R283 5@ 33_0402_5%-D CLK_PCIE_L0M <30>

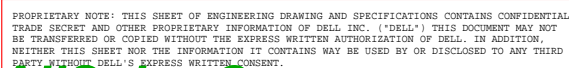
SRCC4 R282 5@ 33_0402_5%-D >>CLK_PCIE_L0M# <30>

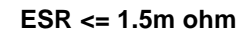
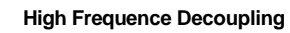


4 GNSRC

SR02 33_0402_5%-D K270 53 PCIE_EXP_CARD#1 2 CLK_PCIE_EXP_CARD# CLK_PCIE_EXP_CARD# <34>

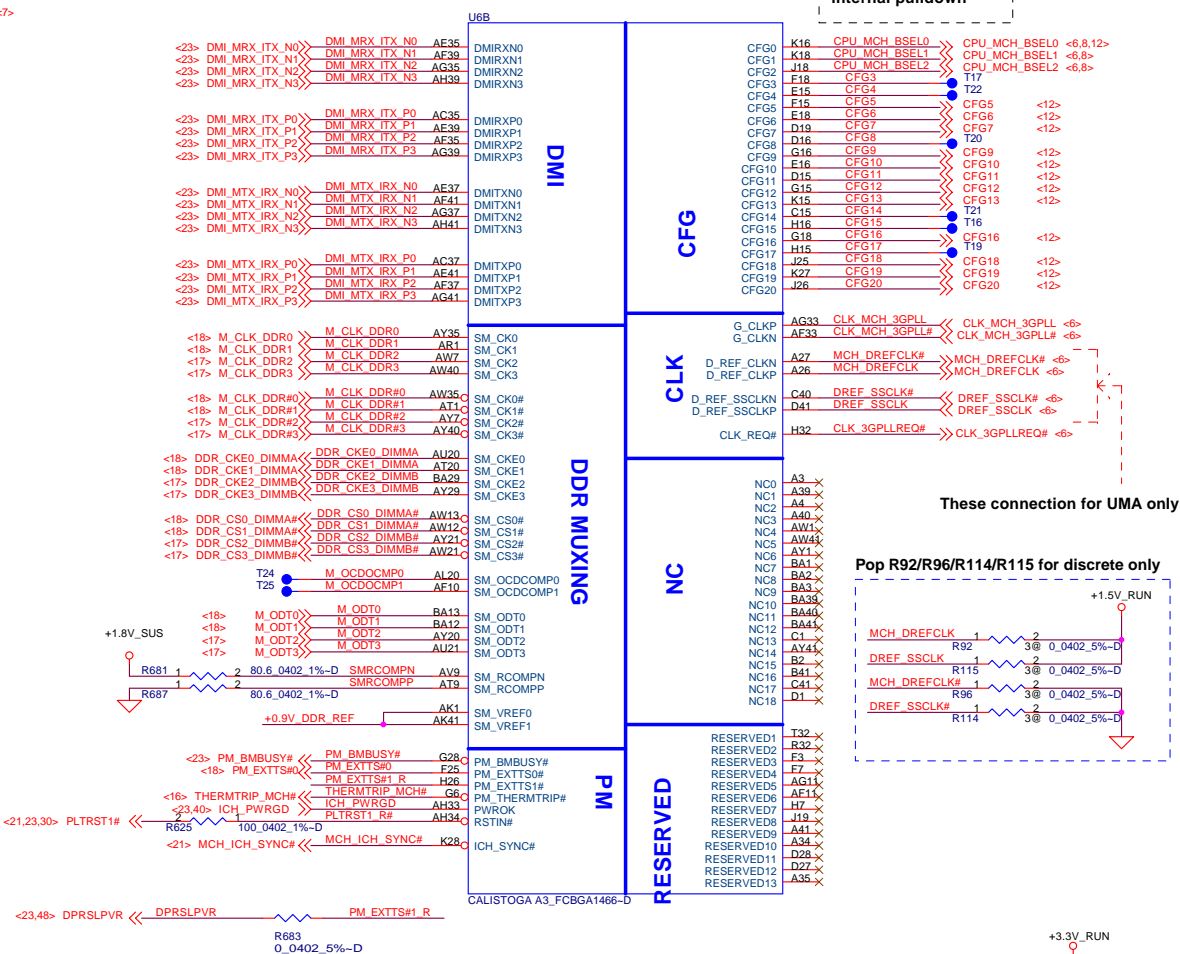
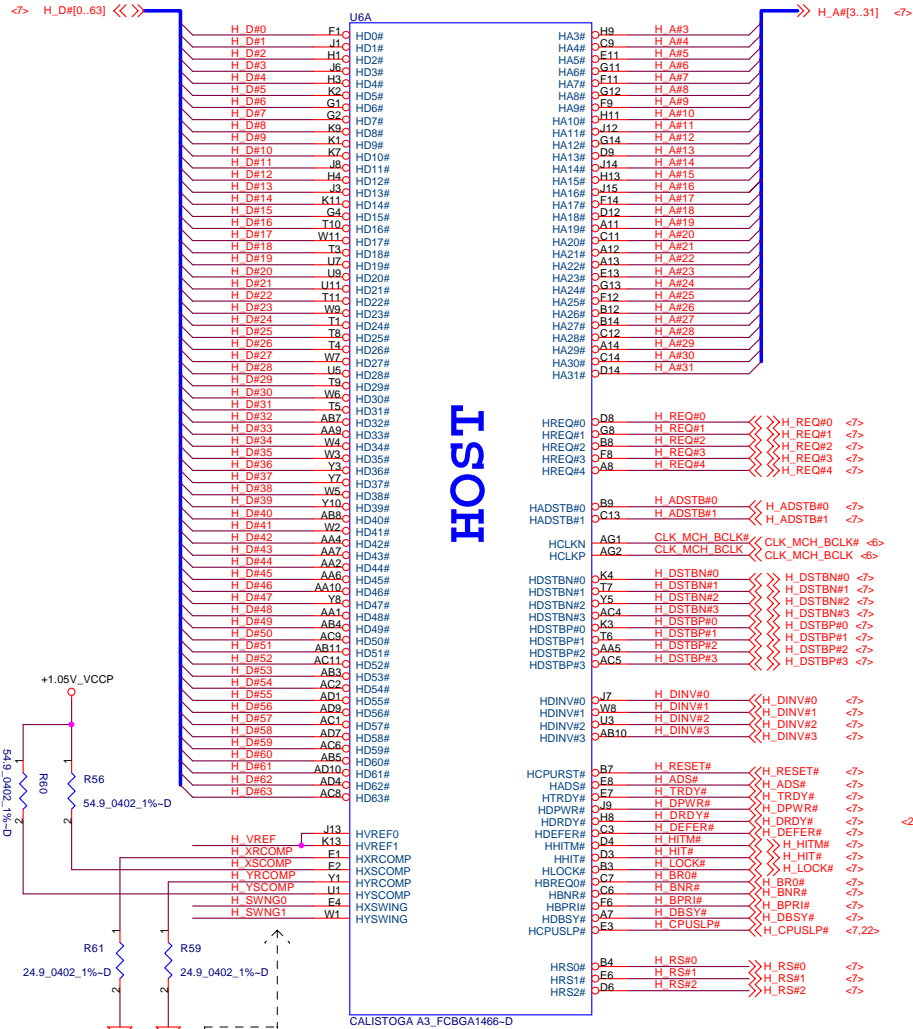




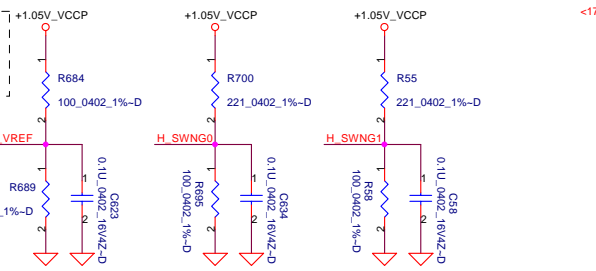


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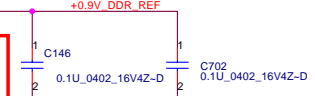
Description at page12
Note :
CFG3:17 has
internal pullup,
CFG18:19 has
internal pulldown



Layout Note:
H_XRCOMP & H_YRCOMP / H_SWNG0 &
H_SWNG1 trace width and spacing is 10/2



Place Close To
AK1 and AK41



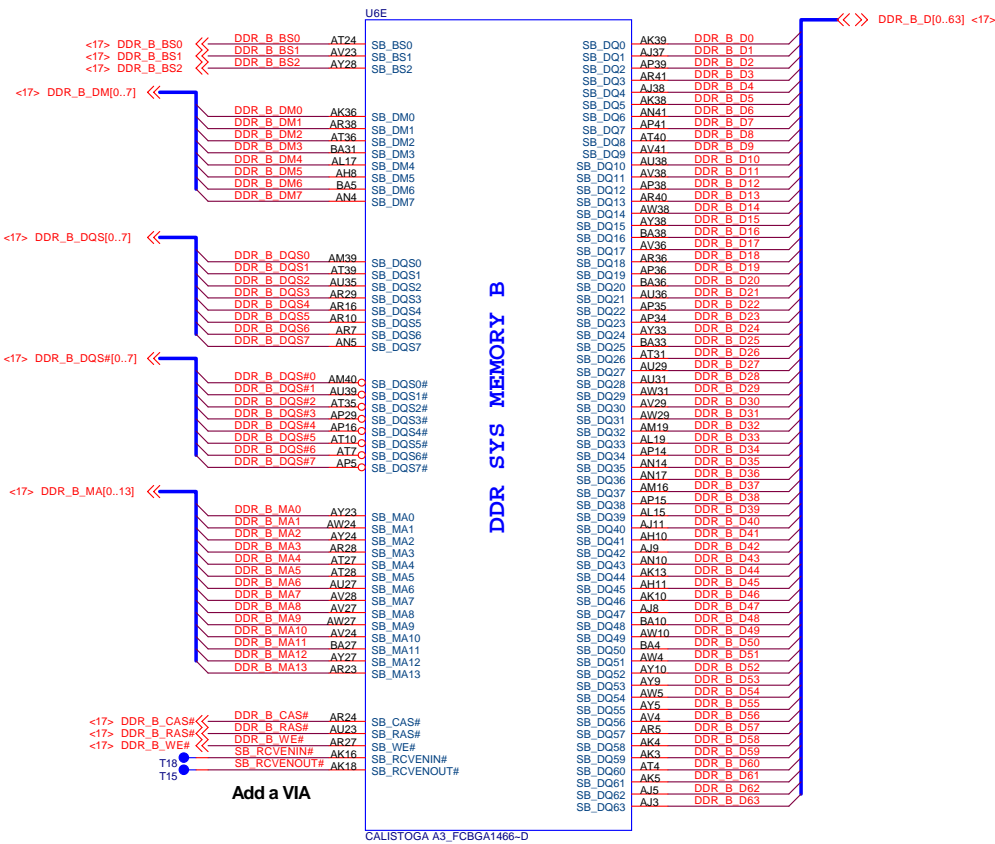
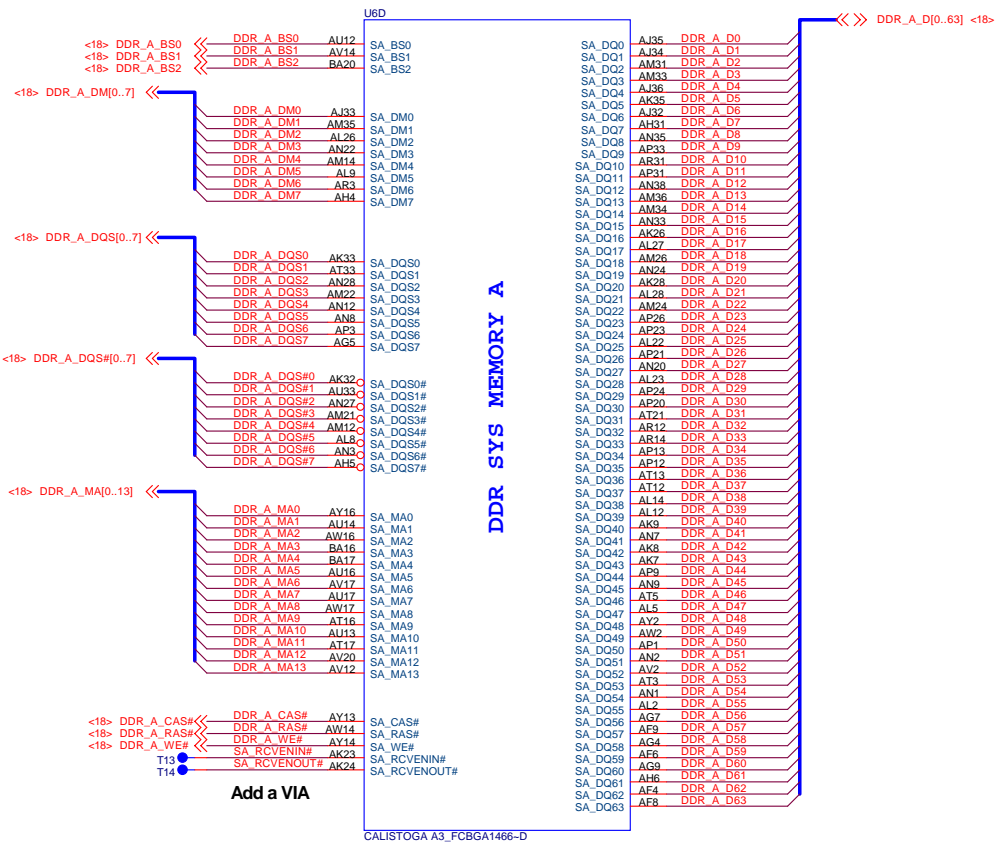
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DDR SYS MEMORY A

DDR SYS MEMORY B

CALISTOGA A3_FCBGA1466-D

CALISTOGA A3_FCBGA1466-D

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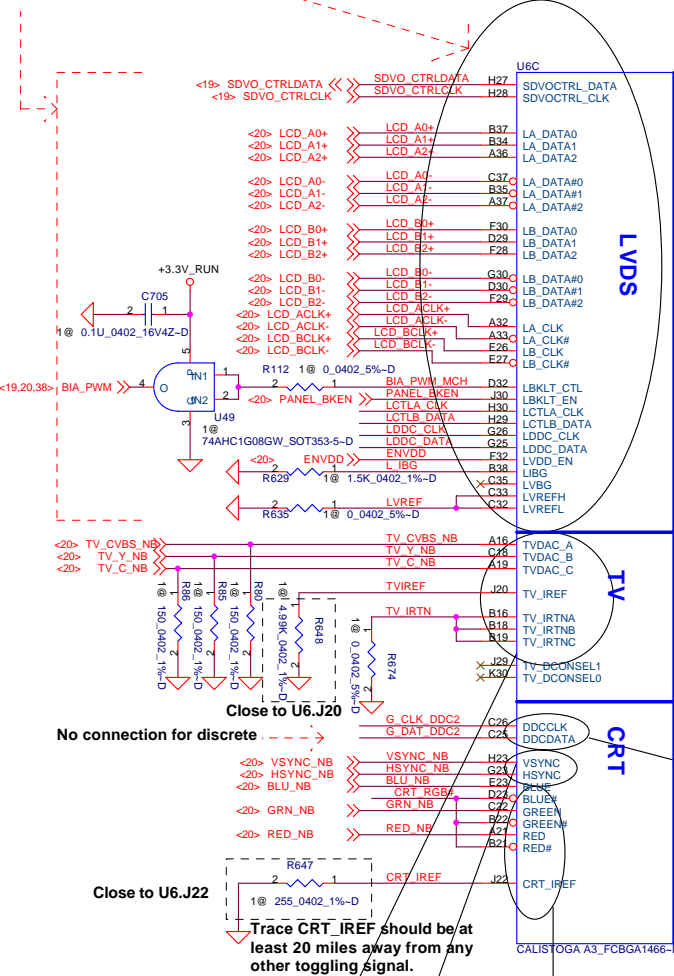
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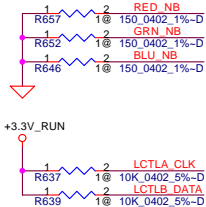
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No connection for discrete

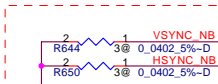


PCI-EXPRESS GRAPHICS

NOTE:
1@ is for UMA Implementation.
3@ is for Discrete Implementation.



Connect to GND for discrete



Note :
CFG3:17 has internal pullup,
CFG18:19 has internal pulldown

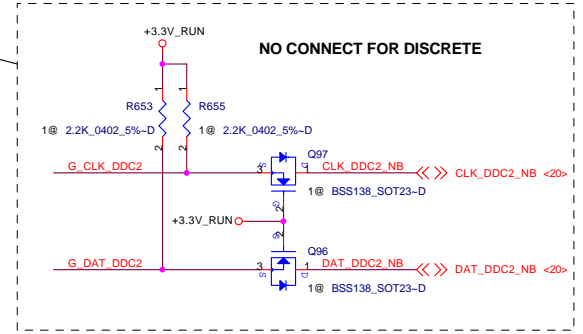
Strap Pin Table

CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = Moby Dick High = Calistoga *
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG10	Low = Reserved High = Mobility *
CFG11	Low = Calistoga * High = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (DMI Lane Reversal)	Low = Normal Operation (Default): * Lane number in Order High = Reverse Lane
SDVO_CTRLDATA	Low = No SDVO Device Present (Default) * High = SDVO Device Present
CFG20 (PCIe/SDVO select)	Low = Only PCIe or SDVO is operational. (Default) * High = PCIe/SDVO are operating simu.

CFG[3:17] have internal pullup

CFG[18:19] have internal pulldown

NOTE: For A Platform That Support Both Integrated and Down Video Solution, A Translation Circuit Could Be Needed At LDDC_CLK and LDDC_DATA signals.



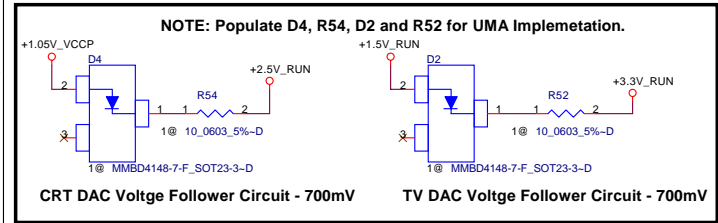
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U6I			AE34		
AC41	VSS0	VSS100	AC34		
AA41	VSS1	VSS101	C34		
W41	VSS2	VSS102	AW33		
T41	VSS3	VSS103	AV33		
P41	VSS4	VSS104	AR33		
M41	VSS5	VSS105	AE33		
J41	VSS6	VSS106	AB33		
F41	VSS7	VSS107	V33		
AY40	VSS8	VSS108	T33		
AP40	VSS9	VSS109	R33		
AN40	VSS10	VSS110	P33		
AK40	VSS11	VSS111	M33		
AJ40	VSS12	VSS112	H33		
AH40	VSS13	VSS113	G33		
AG40	VSS14	VSS114	F33		
AF40	VSS15	VSS115	D33		
AE40	VSS16	VSS116	C33		
AD40	VSS17	VSS117	B33		
AC39	VSS18	VSS118	AH32		
AB39	VSS19	VSS119	AG32		
AA39	VSS20	VSS120	AF32		
AY39	VSS21	VSS121	AE32		
AP39	VSS22	VSS122	AC32		
AN39	VSS23	VSS123	AB32		
AK39	VSS24	VSS124	G32		
AJ39	VSS25	VSS125	AY31		
AH39	VSS26	VSS126	AV31		
AG39	VSS27	VSS127	AN31		
AF39	VSS28	VSS128	AJ31		
AE39	VSS29	VSS129	AG31		
AD39	VSS30	VSS130	AB31		
AC39	VSS31	VSS131	Y31		
AB39	VSS32	VSS132	AB30		
AA39	VSS33	VSS133	E30		
AY39	VSS34	VSS134	AT29		
AP39	VSS35	VSS135	AN29		
AN39	VSS36	VSS136	AB29		
AK39	VSS37	VSS137	T29		
AJ39	VSS38	VSS138	N29		
AH39	VSS39	VSS139	K29		
AG39	VSS40	VSS140	G29		
AF39	VSS41	VSS141	E29		
AE39	VSS42	VSS142	C29		
AD39	VSS43	VSS143	B29		
AC39	VSS44	VSS144	A29		
AB39	VSS45	VSS145	BA28		
AA39	VSS46	VSS146	AW28		
AY39	VSS47	VSS147	AU28		
AP39	VSS48	VSS148	AP28		
AN39	VSS49	VSS149	AM28		
AK39	VSS50	VSS150	AD28		
AJ39	VSS51	VSS151	AC28		
AH39	VSS52	VSS152	W28		
AG39	VSS53	VSS153	J28		
AF39	VSS54	VSS154	E28		
AE39	VSS55	VSS155	AP27		
AD39	VSS56	VSS156	AM27		
AC39	VSS57	VSS157	AK27		
AB39	VSS58	VSS158	J27		
AA39	VSS59	VSS159	G27		
AY39	VSS60	VSS160	F27		
AP39	VSS61	VSS161	C27		
AN39	VSS62	VSS162	B27		
AK39	VSS63	VSS163	AN26		
AJ39	VSS64	VSS164	M26		
AH39	VSS65	VSS165	K26		
AG39	VSS66	VSS166	D26		
AF39	VSS67	VSS167	AK25		
AE39	VSS68	VSS168	P25		
AD39	VSS69	VSS169	K25		
AC39	VSS70	VSS170	H25		
AB39	VSS71	VSS171	E25		
AA39	VSS72	VSS172	D25		
AY39	VSS73	VSS173	A25		
AP39	VSS74	VSS174	BA24		
AN39	VSS75	VSS175	AU24		
AK39	VSS76	VSS176	AL24		
AJ39	VSS77	VSS177	AW23		
AH39	VSS78	VSS178	AT23		
AG39	VSS79	VSS179	AN23		
AF39	VSS80	VSS180	AM23		
AE39	VSS81	VSS181	AH23		
AD39	VSS82	VSS182	AC23		
AC39	VSS83	VSS183	W23		
AB39	VSS84	VSS184	K23		
AA39	VSS85	VSS185	J23		
AY39	VSS86	VSS186	C23		
AP39	VSS87	VSS187	AA22		
AN39	VSS88	VSS188	K22		
AK39	VSS89	VSS189	C22		
AJ39	VSS90	VSS190	F22		
AH39	VSS91	VSS191	E22		
AG39	VSS92	VSS192	D22		
AF39	VSS93	VSS193	A22		
AE39	VSS94	VSS194	BA21		
AD39	VSS95	VSS195	AV21		
AC39	VSS96	VSS196	AR21		
AB39	VSS97	VSS197			
AA39	VSS98	VSS198			
AY39	VSS99	VSS199			

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U6J			AG10		
AN21	VSS200	VSS280	AC10		
AL21	VSS201	VSS281	W10		
AB21	VSS202	VSS282	U10		
Y21	VSS203	VSS283	BA9		
P21	VSS204	VSS284	AW9		
K21	VSS205	VSS285	AR9		
J21	VSS206	VSS286	AH9		
H21	VSS207	VSS287	AB9		
C21	VSS208	VSS288	Y9		
AW20	VSS209	VSS289	R9		
AR20	VSS210	VSS290	G9		
AM20	VSS211	VSS291	E9		
AA20	VSS212	VSS292	AG8		
K20	VSS213	VSS293	AD8		
B20	VSS214	VSS294	AA8		
A20	VSS215	VSS295	U8		
AC19	VSS216	VSS296	K8		
W19	VSS217	VSS297	C8		
K19	VSS218	VSS298	BA7		
G19	VSS219	VSS299	AV7		
C19	VSS220	VSS300	AF7		
AH18	VSS221	VSS301	AL7		
P18	VSS222	VSS302	AJ7		
H18	VSS223	VSS303	AE7		
D18	VSS224	VSS304	AC7		
A18	VSS225	VSS305	R7		
AY17	VSS226	VSS306	G7		
AR17	VSS227	VSS307	D7		
AP17	VSS228	VSS308	AG6		
AM17	VSS229	VSS309	AD6		
AK17	VSS230	VSS310	AB6		
AV16	VSS231	VSS311	Y6		
AN16	VSS232	VSS312	U6		
W16	VSS233	VSS313	N6		
J16	VSS234	VSS314	K6		
F16	VSS235	VSS315	H6		
C16	VSS236	VSS316	B6		
AW15	VSS237	VSS317	AV5		
AM15	VSS238	VSS318	AF5		
AK15	VSS239	VSS319	AD5		
N15	VSS240	VSS320	AY4		
M15	VSS241	VSS321	AR4		
L15	VSS242	VSS322	AP4		
B15	VSS243	VSS323	AL4		
A15	VSS244	VSS324	AJ4		
BA14	VSS245	VSS325	Y4		
E14	VSS246	VSS326	U4		
AT14	VSS247	VSS327	R4		
AK14	VSS248	VSS328	F4		
AD14	VSS249	VSS329	C4		
AA14	VSS250	VSS330	AY3		
W14	VSS251	VSS331	AW3		
K14	VSS252	VSS332	AV3		
H14	VSS253	VSS333	AL3		
E14	VSS254	VSS334	AH3		
AV13	VSS255	VSS335	AG3		
AR13	VSS256	VSS336	AD3		
AM13	VSS257	VSS337	AC3		
AK13	VSS258	VSS338	AA3		
AG13	VSS259	VSS339	G3		
P13	VSS260	VSS340	AT2		
F13	VSS261	VSS341	AR2		
D13	VSS262	VSS342	AP2		
B13	VSS263	VSS343	AJ2		
AY12	VSS264	VSS344	AD2		
AC12	VSS265	VSS345	AB2		
K12	VSS266	VSS346	Y2		
H12	VSS267	VSS347	U2		
E12	VSS268	VSS348	T2		
AT11	VSS269	VSS349	N2		
AK11	VSS270	VSS350	H2		
AD11	VSS271	VSS351	F2		
AA11	VSS272	VSS352	C2		
W11	VSS273	VSS353	AL1		
K11	VSS274	VSS354			
B11	VSS275	VSS355			
AV10	VSS276	VSS356			
AP10	VSS277	VSS357			
AL10	VSS278	VSS358			
AJ10	VSS279	VSS359			
		VSS360			

CALISTOGA A3_FCBGA1466-D

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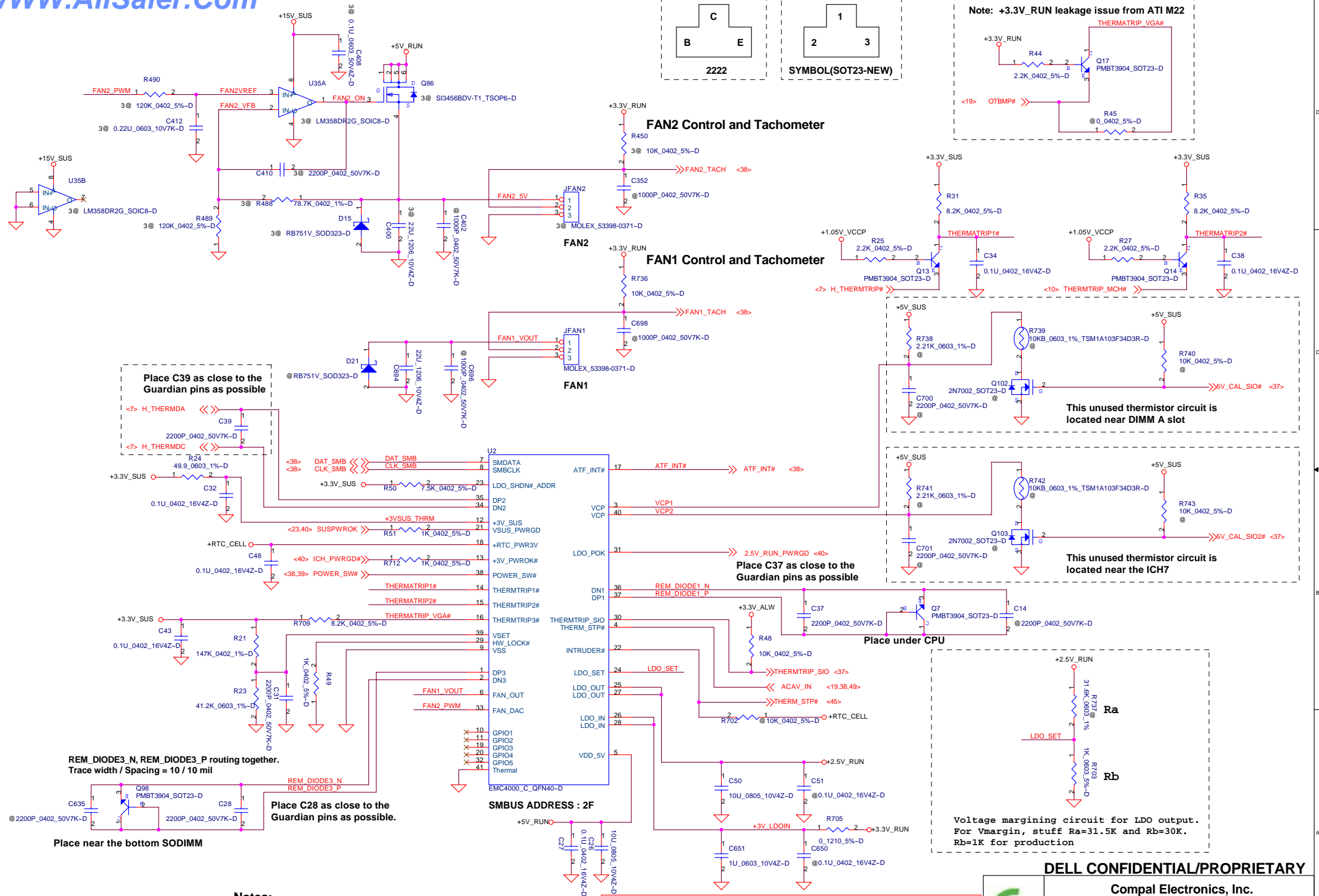
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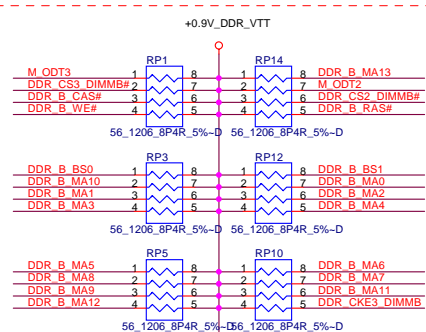
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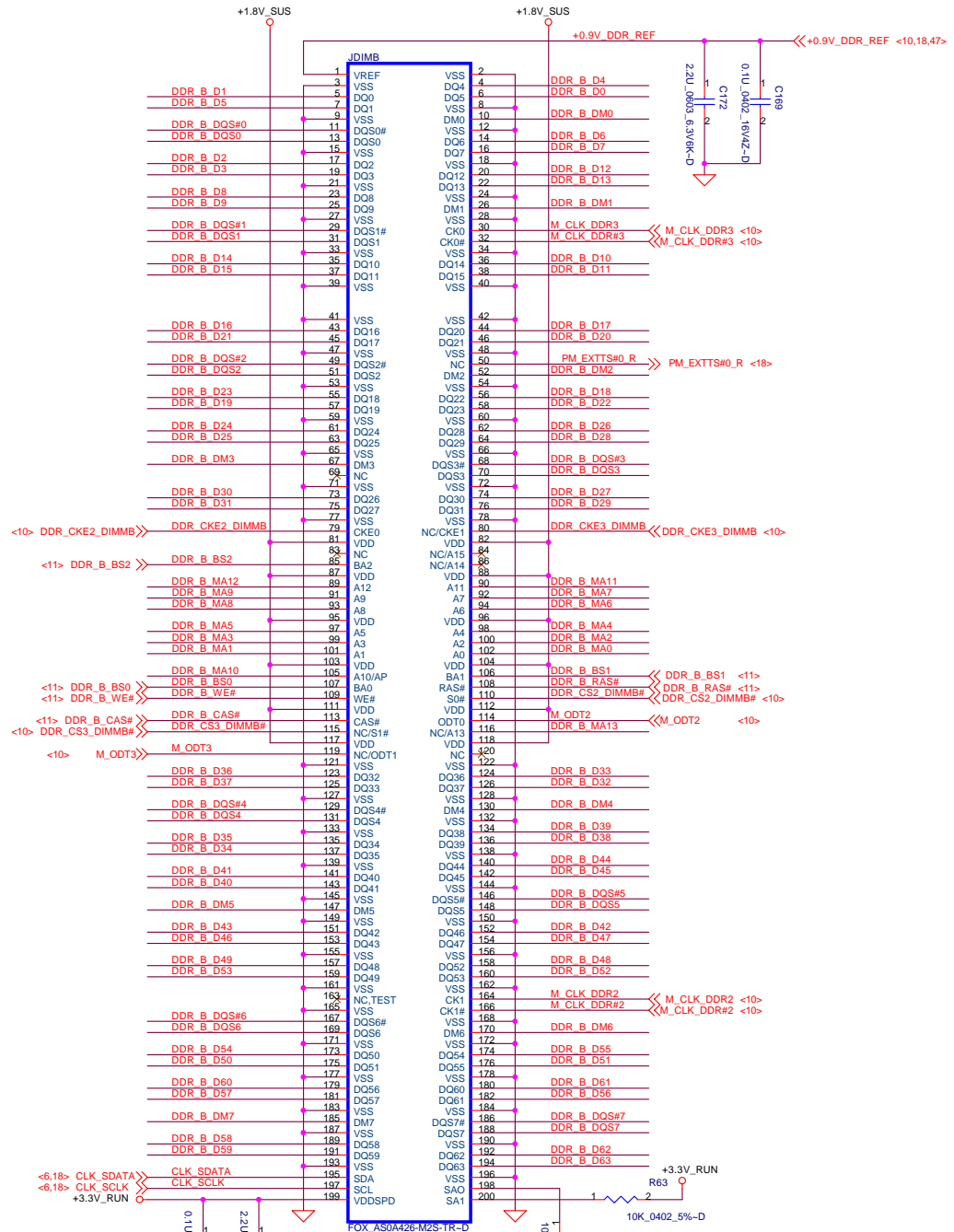


Notes:
"Solder thermal pad to plane. Add 9 ground vias to pad."

The diagram illustrates the power plane for +0.9V_DDR_VTT. It features a series of capacitors (C139 to C596) connected to a common ground rail. Each capacitor is labeled with its value: 0.1uF, 0.002, 16V/AZ-D. The capacitors are connected to a top rail labeled +0.9V_DDR_VTT. A red arrow points to the bottom rail, which is labeled 0.1uF, 0.002, 16V/AZ-D.



Layout Note:
Place these resistor closely JDIMB,all trace length



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Compal Electronics, Inc.

DDRII-SODIMM SLOT-B

Document Number
LA-2881P

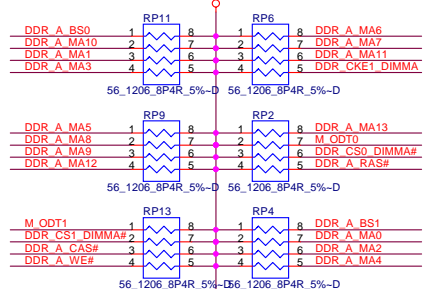
Date: Tuesday, December 13, 2005 Sheet 17 of 62

The schematic diagram illustrates a 10-bit DAC implementation. It features a 10x2 multiplexer (MUX) and a 10-bit DAC IC. The MUX is configured with its 10 data inputs (D0-D9) connected to the DAC's 10-bit digital input (A[9:0]). The MUX's 2 data outputs (Y0-Y1) are connected to the DAC's 2-bit digital output (B[1:0]). The MUX's 10 control inputs (S0-S9) are connected to the DAC's 10-bit control input (C[9:0]). The MUX's 2 control inputs (S10-S11) are connected to the DAC's 2-bit control input (D[1:0]). The MUX's 10 data inputs (D0-D9) are connected to the DAC's 10-bit digital input (A[9:0]). The MUX's 2 data outputs (Y0-Y1) are connected to the DAC's 2-bit digital output (B[1:0]). The MUX's 10 control inputs (S0-S9) are connected to the DAC's 10-bit control input (C[9:0]). The MUX's 2 control inputs (S10-S11) are connected to the DAC's 2-bit control input (D[1:0]).

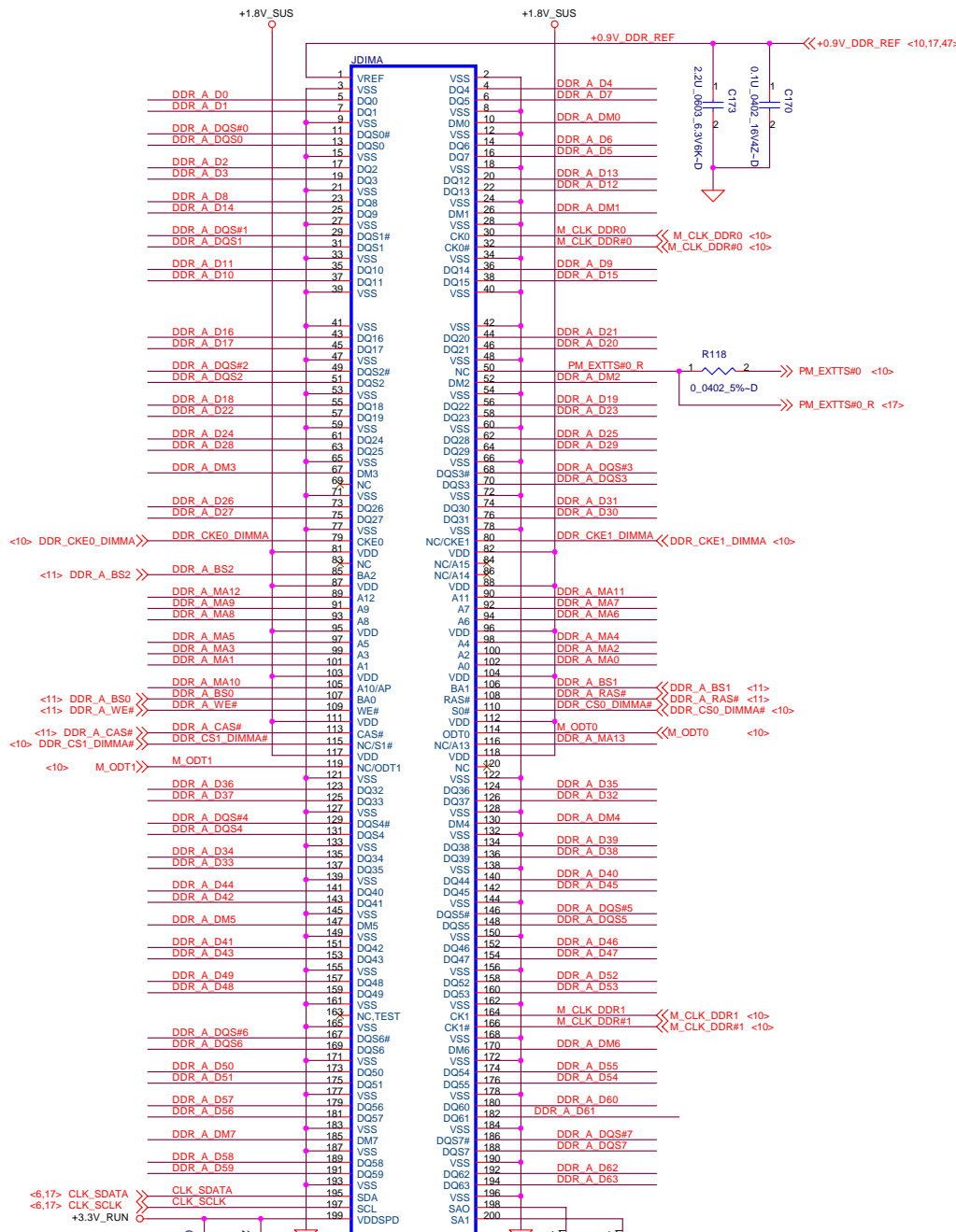
The diagram illustrates the power plane for +0.9V_DDR_VTT. It features a series of capacitors connected to a common ground plane. The capacitors are labeled as follows:

- C395: 0.1uF, 0.002, 16V/AZ-D
- C59: 0.1uF, 0.002, 16V/AZ-D
- C573: 0.1uF, 0.002, 16V/AZ-D
- C585: 0.1uF, 0.002, 16V/AZ-D
- C582: 0.1uF, 0.002, 16V/AZ-D
- C577: 0.1uF, 0.002, 16V/AZ-D
- C574: 0.1uF, 0.002, 16V/AZ-D
- C139: 0.1uF, 0.002, 16V/AZ-D
- C135: 0.1uF, 0.002, 16V/AZ-D
- C126: 0.1uF, 0.002, 16V/AZ-D
- C122: 0.1uF, 0.002, 16V/AZ-D
- C116: 0.1uF, 0.002, 16V/AZ-D
- C111: 0.1uF, 0.002, 16V/AZ-D

The capacitors are connected to a common ground plane, which is indicated by a red arrow pointing to the ground symbol at the bottom right. The entire schematic is enclosed in a dashed red box.



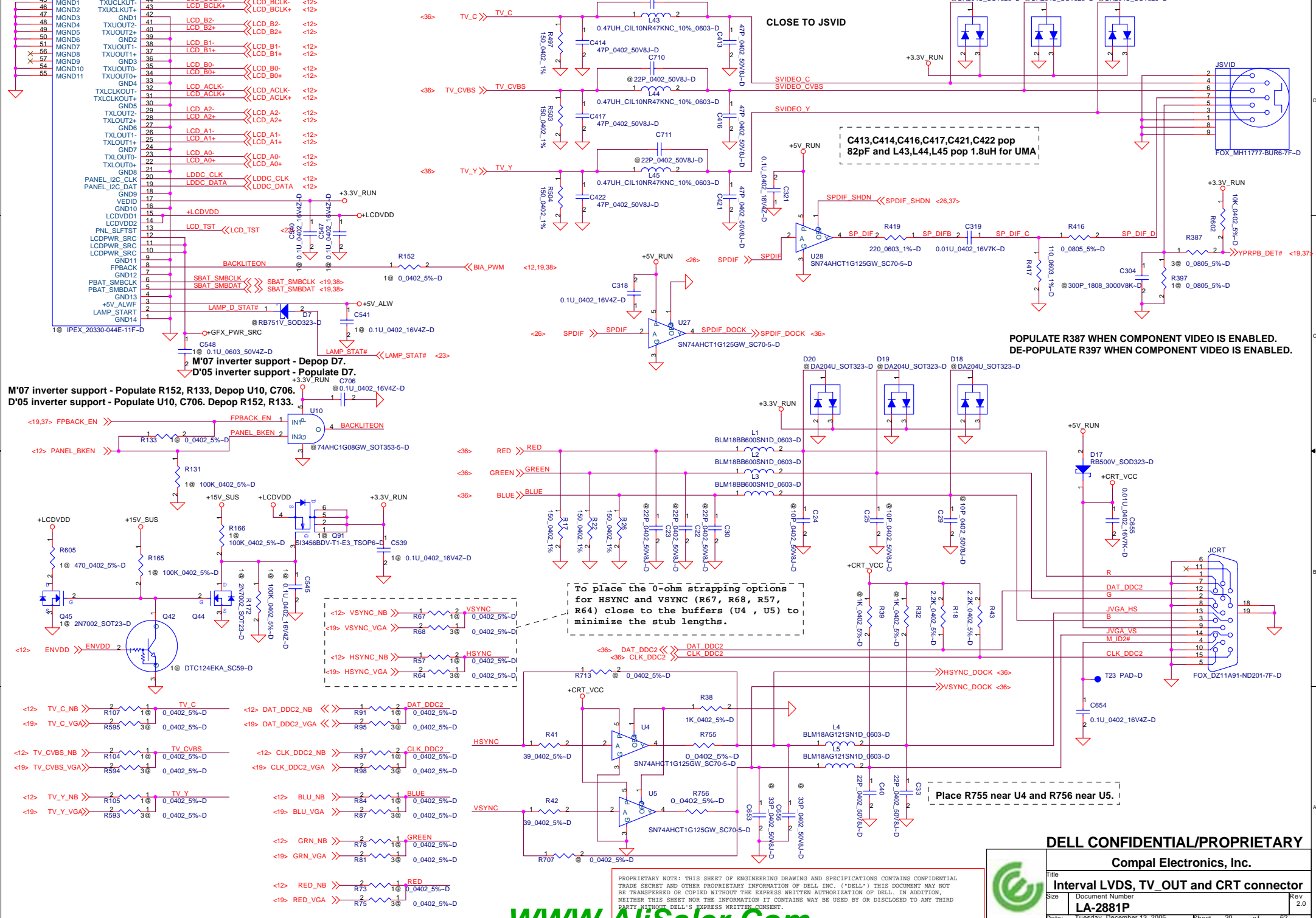
Layout Note:
Place these resistor
closely JDIMA,all
trace length



Size	Document Number	Rev
	LA-2881P	2.0
Date:	Tuesday, December 13, 2005	Sheet 18 of 62

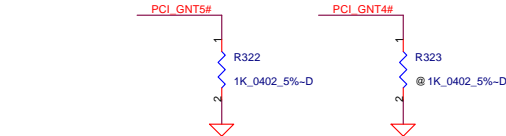
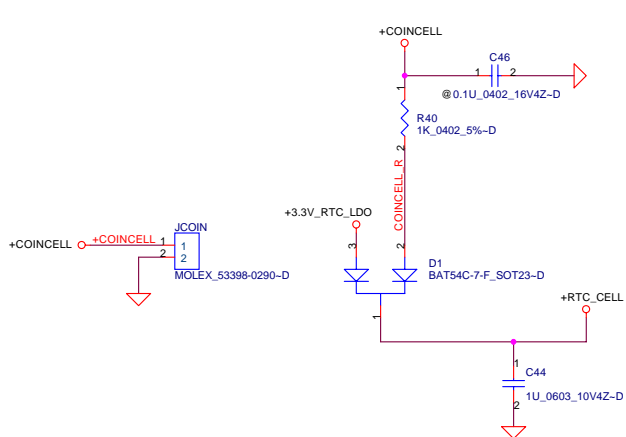
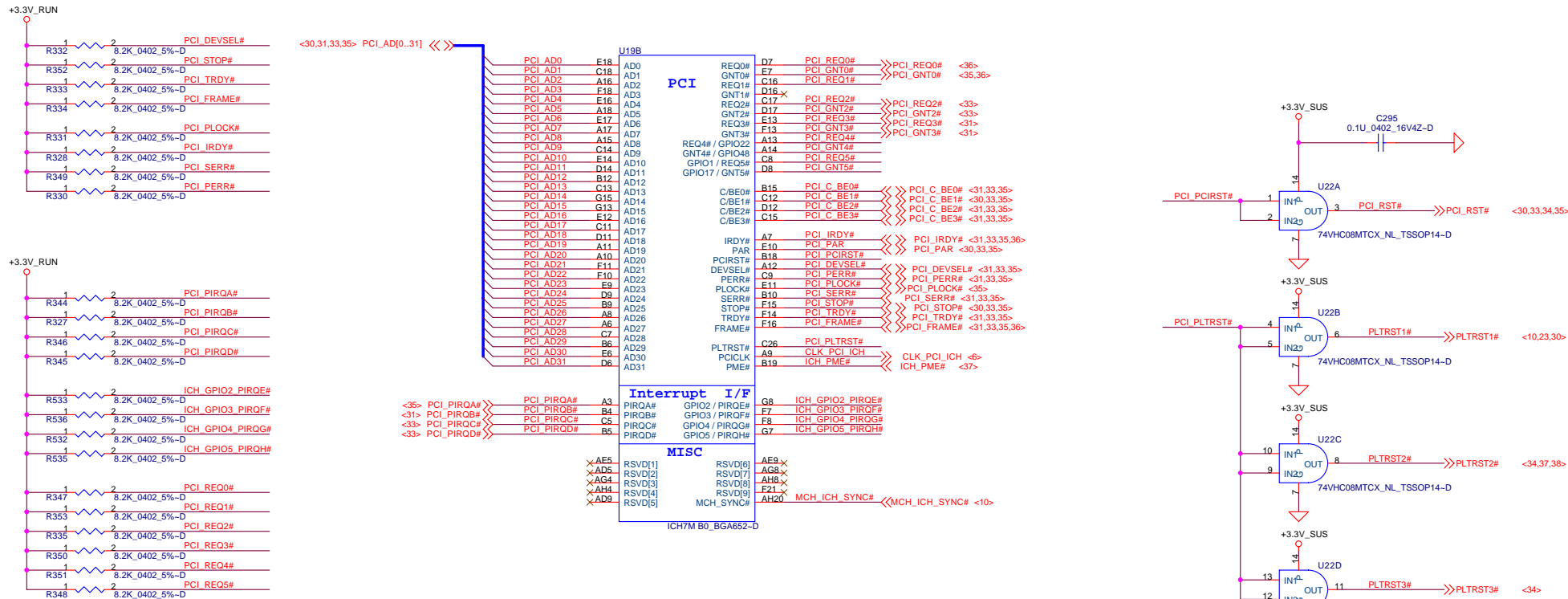


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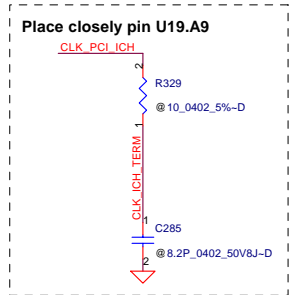
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Compal Electronics, Inc.	
Title	Interval LVDS, TV_OUT and CRT connector
Size	Document Number
LA-2881P	
Date	Rev
Tuesday, December 13, 2005	2.0
Sheet	of
20	62



ICH Boot BIOS select

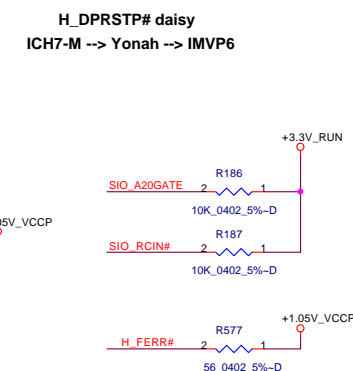
		GNT5# R322	GNT4# R323
LPC	11	unstuff	unstuff
PCI	10	unstuff	stuff
SPI	01	stuff	unstuff



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Compal Electronics, Inc.	
Title ICH7-M(1/4)	
Size	Document Number LA-2881P
Date	Rev 2.0

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LA-2881P

Date: Tuesday, December 13, 2005 Sheet 22 of 62

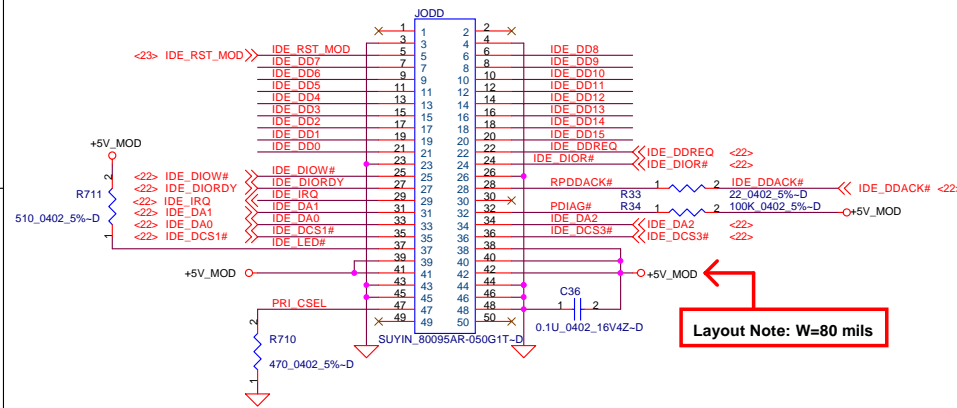
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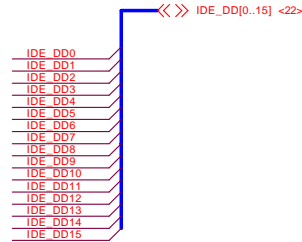
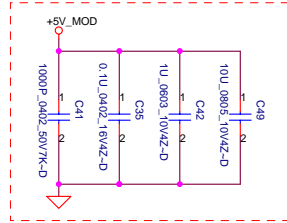
Date:	Tuesday, December 13, 2005	Sheet	24	of	62
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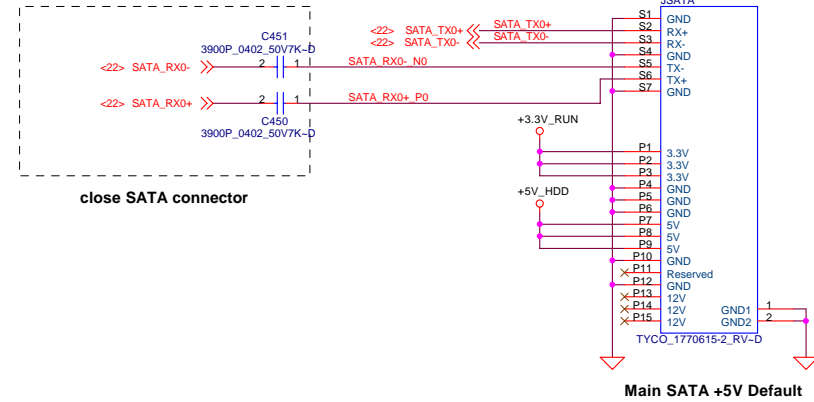
CD-ROM Connector



Layout Note: Place close to CD-ROM CONN

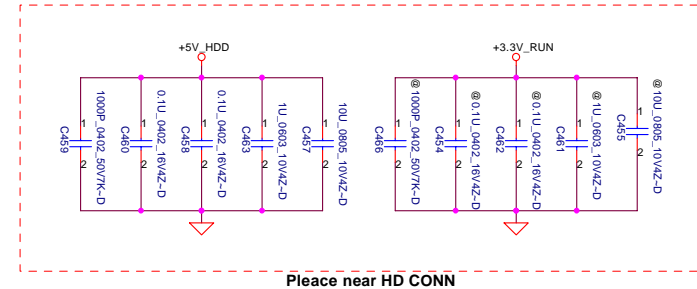


SATA Connector



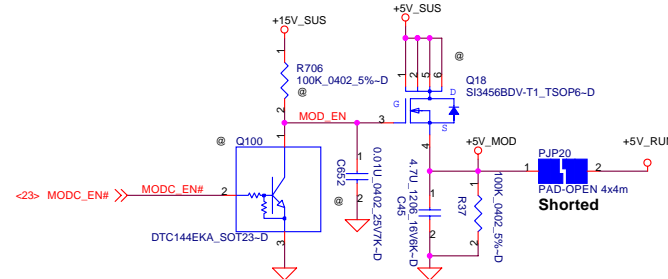
close SATA connector

Main SATA +5V Default

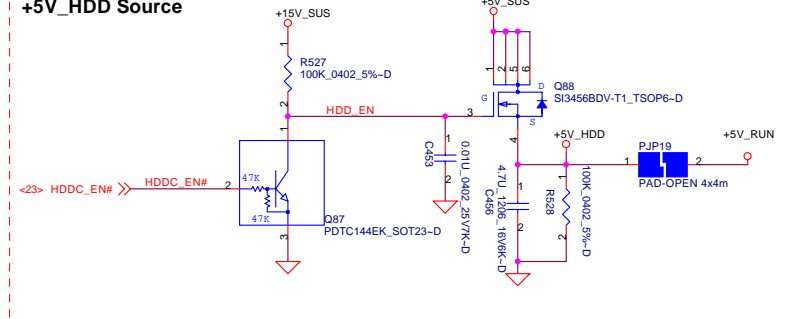


Place near HD CONN

+5V_MOD Source



+5V_HDD Source

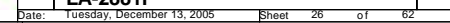


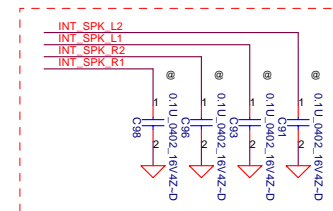
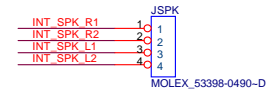
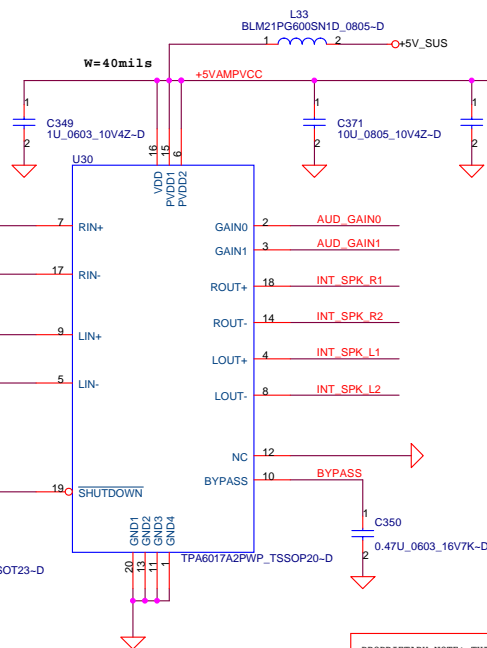
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Title		SATA HDD and CD-ROM CONN.	
Size	Document Number	LA-2881P	
Date	1uesday, December 13, 2005	Sheet	25 of 62

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	GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
	0	0	6dB	90K ohm
	0	1	10dB	70K ohm
	1	0	15.6dB	45K ohm
*	1	1	21.6dB	25K ohm

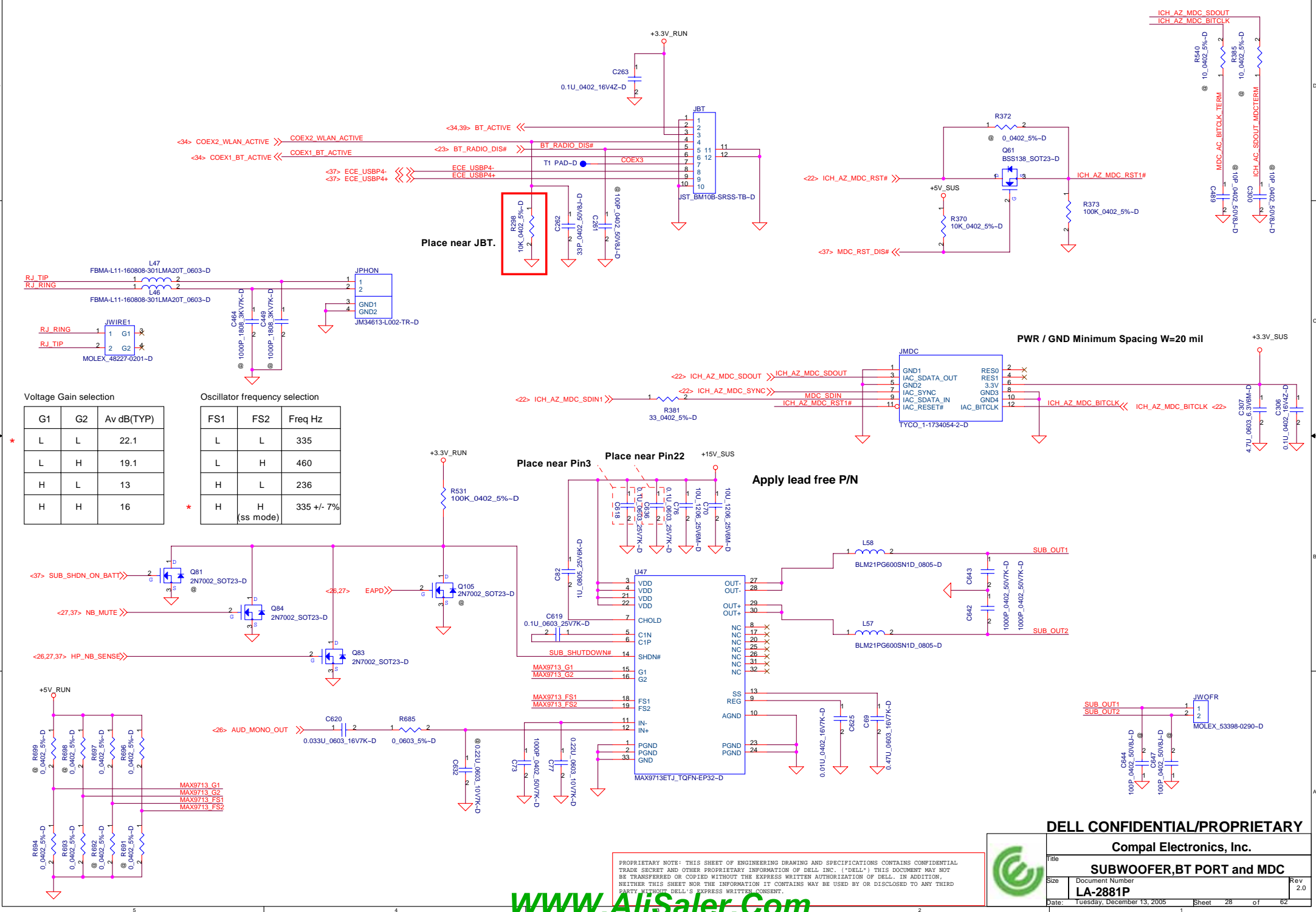
	Compal Electronics, Inc.
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Amplifier and Phone Jack

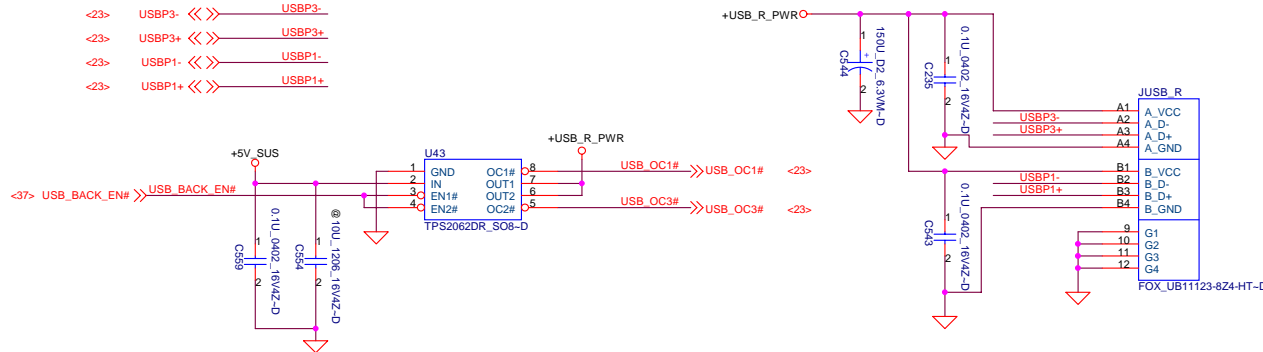
Size	Document Number
	LA-2881P

Date: Tuesday, December 13, 2005 Sheet 27 of 62

Date:	Tuesday, December 16, 2008	Sheet	27	91	92
	1				

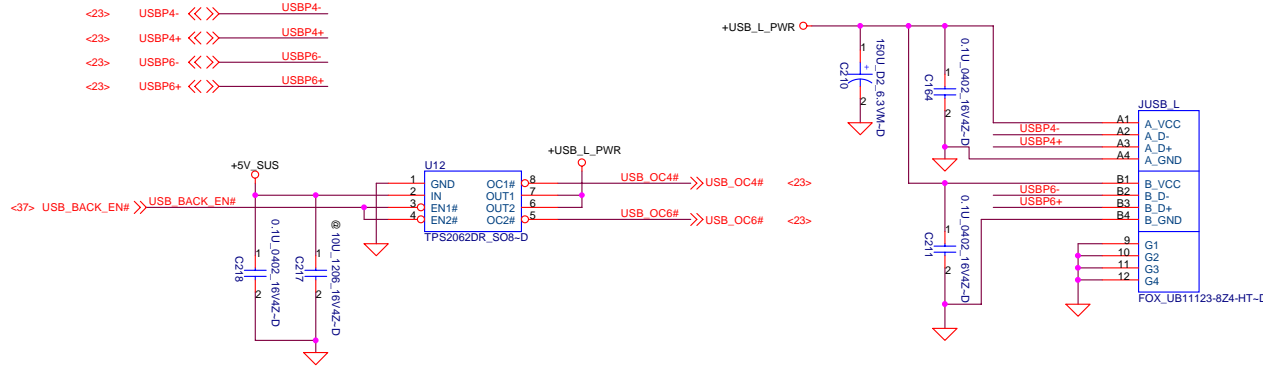


Ext Back Right USB Port

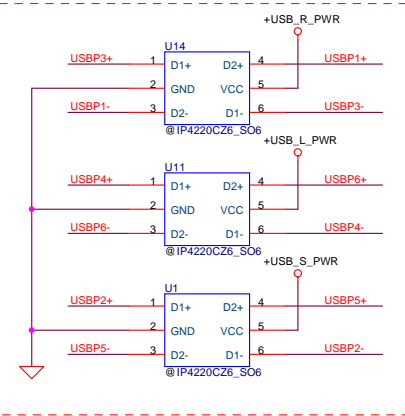


USB IO PORT#	DESTINATION
1	JUSB_R (Ext Back Right Bottom)
2	JUSB_S (Ext Side Bottom)
3	JUSB_R (Ext Back Right Top)
4	JUSB_L (Ext Back Left Top)
5	JUSB_S (Ext Side Top)
6	JUSB_L (Ext Back Left Bottom)

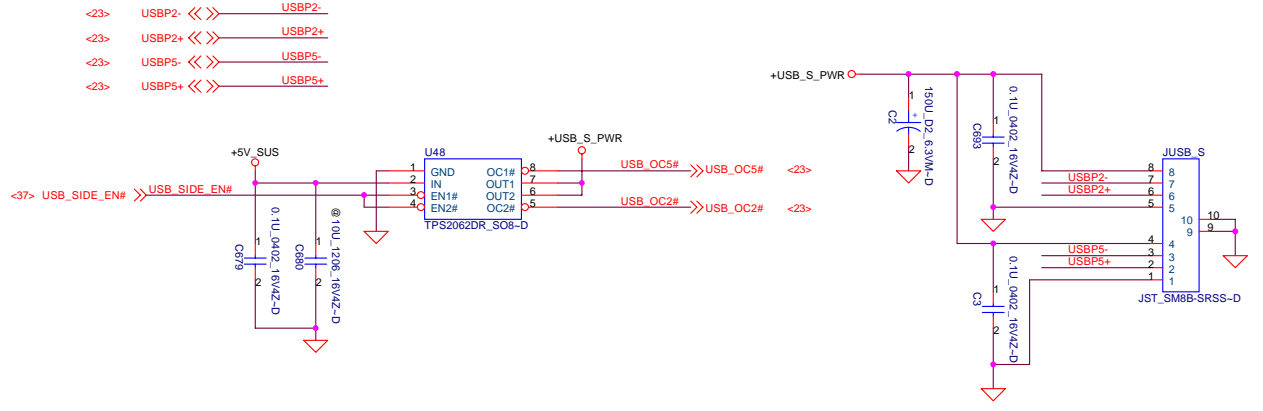
Ext Back Left USB Port



Place U189, U190, U191 as close as USB connector.



Ext Side USB Port



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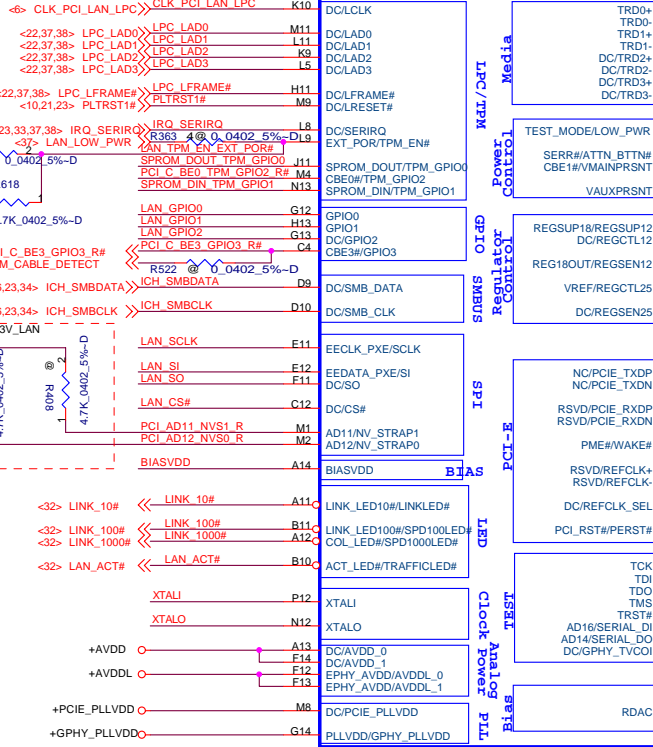
Compal Electronics, Inc.

USB 2.0 PORT

Title	Document Number	Rev
LA-2881P		2.0
Date: Tuesday, December 13, 2005	Sheet 29 of 62	

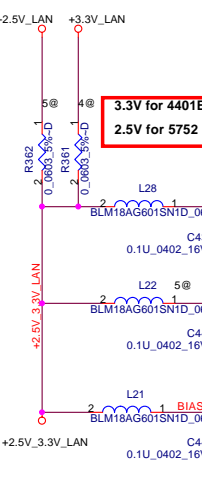
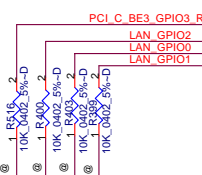
P/N: SA0000071L (5752KFB2); 5@
SA00000D0L (4401E); 4@

BCM4401E/BCM5752

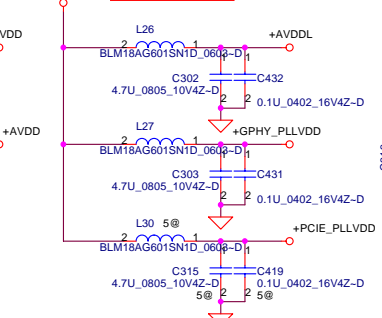


For Rikers:
No POP R612 and POP R498
for disabling TPM

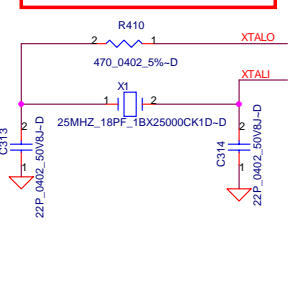
POP option for 5752 NVRAM
(Default EEPROM is ST)



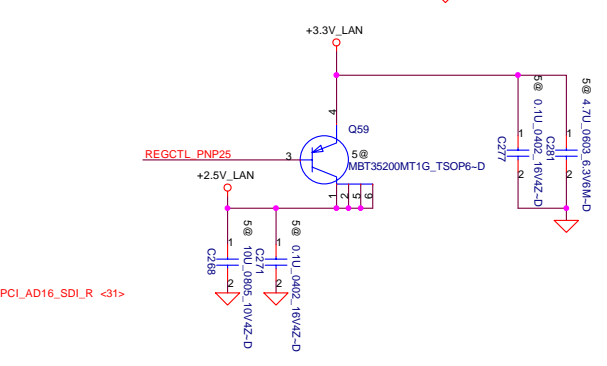
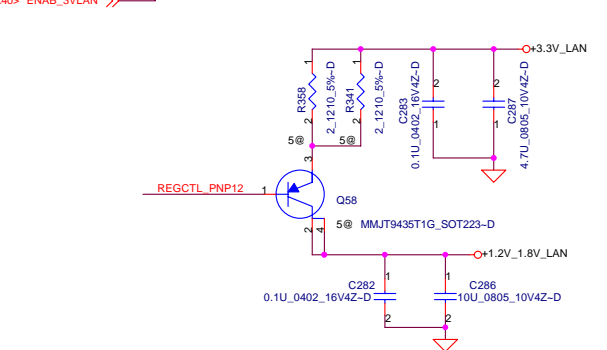
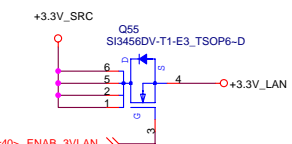
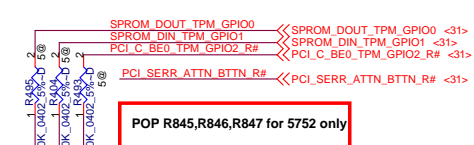
1.8V for 4401E
1.2V for 5752



470 ohm(P/N: SD02847008L) for 5752
750 ohm(P/N: SD02875008L) for 4401E



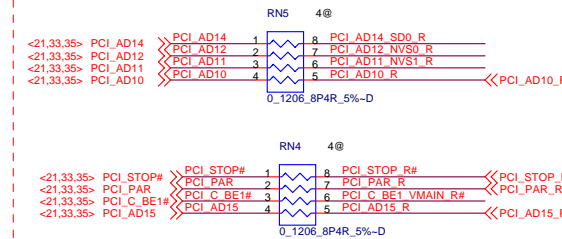
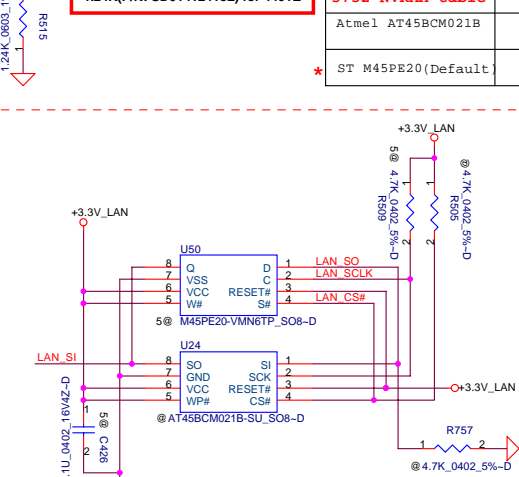
Layout Notice : No high speed signal should be routed near RDAC or on adjacent layer to RDAC



5752 NVRAM , See NVRAM table, Set ST_45PE20 as default

5752 NVRAM table	NV_STRAP1	NV_STRAP0	SO	SI	CS#	SCLK
Atmel AT45BCM021B	0	0	1	0	1	1
* ST M45PE20(Default)	0	1	1	0	0	1

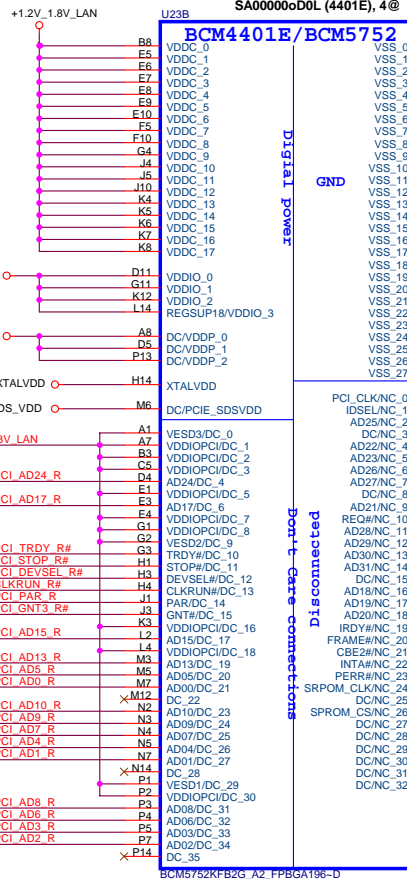
1.15K(P/N: SD01411518L) for 5752
1.24K(P/N: SD01412418L) for 4401E



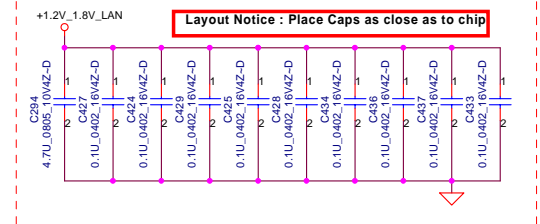
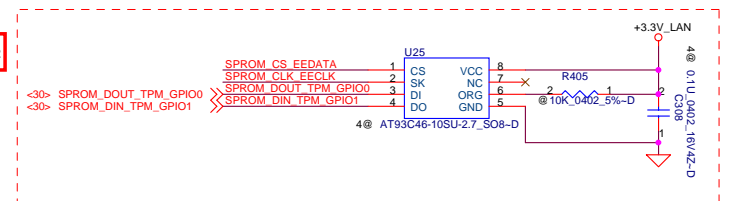
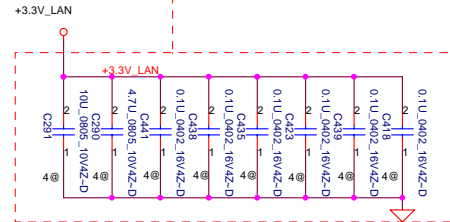
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Compal Electronics, Inc.		
BCM5752/4401E		
Title	Document Number	Rev
	LA-2881P	2.0
Date	Sheet	of
Tuesday, December 13, 2005	30	62

1.8V for 4401E
1.2V for 5752

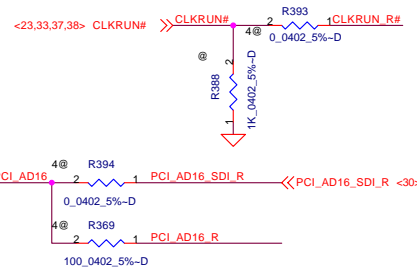


Place as close as to U22B, Pin A1, A7, B3, C5, E1, E4, G1, G2, K3, L4, P1, P2

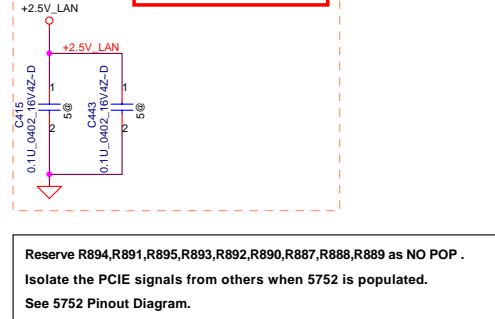


Layout Notice : Place Caps as close as to chip

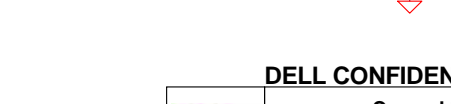
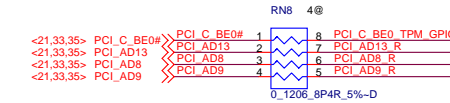
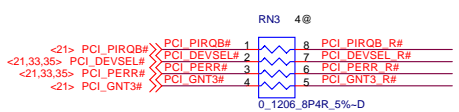
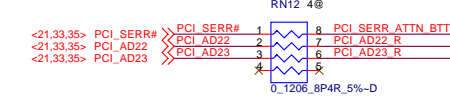
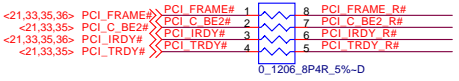
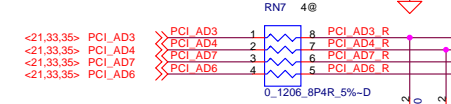
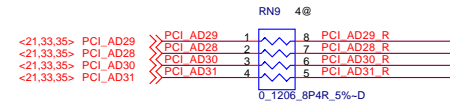
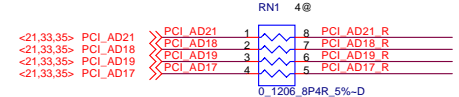
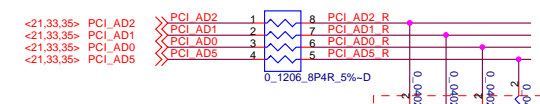
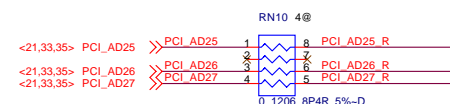
No POP R868
(When CLKRUN# is support in system)



Place as close as to chip
U22, Pin A8, D5, P13



Reserve R894,R891,R895,R893,R892,R890,R887,R888,R889 as NO POP.
Isolate the PCIE signals from others when 5752 is populated.
See 5752 Pinout Diagram.



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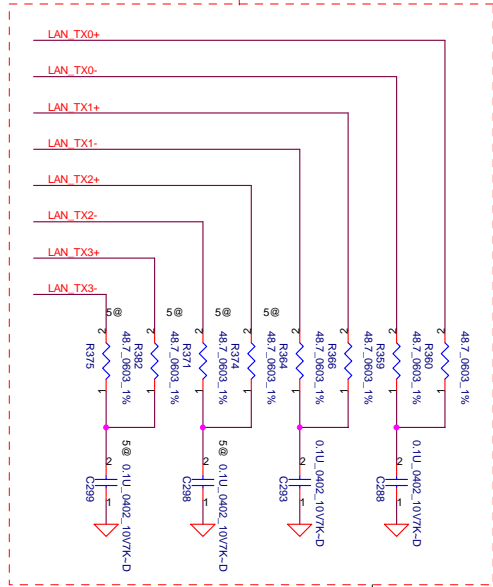
BCM5752/4401E

LA-2881P

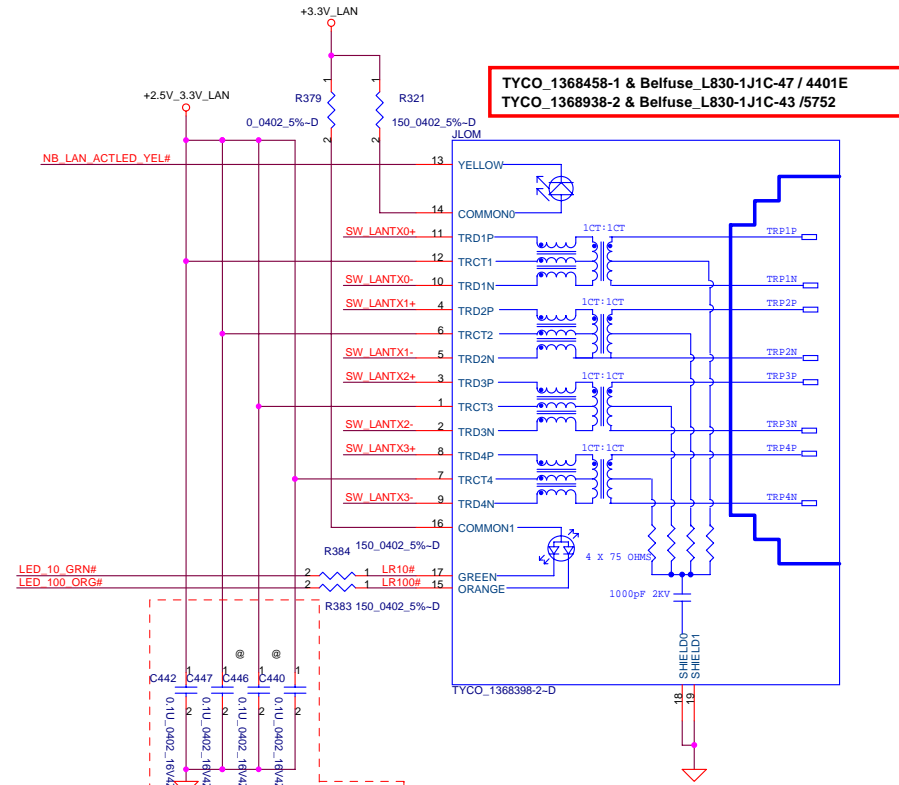
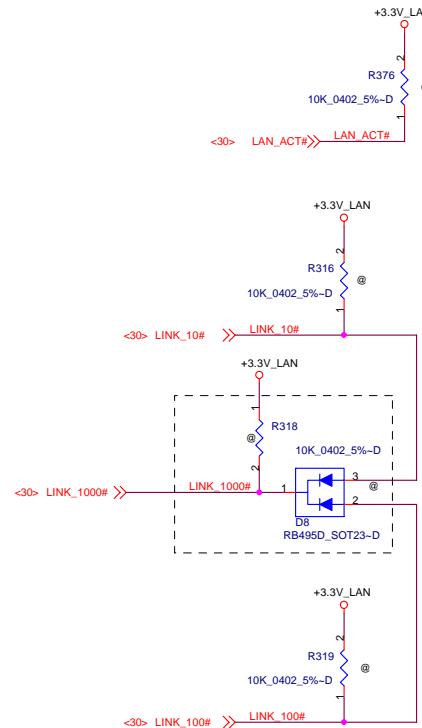
Date: Tuesday, December 13, 2005 Sheet 31 of 62

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Apply lead free P/N
termination as close as
chip as possible

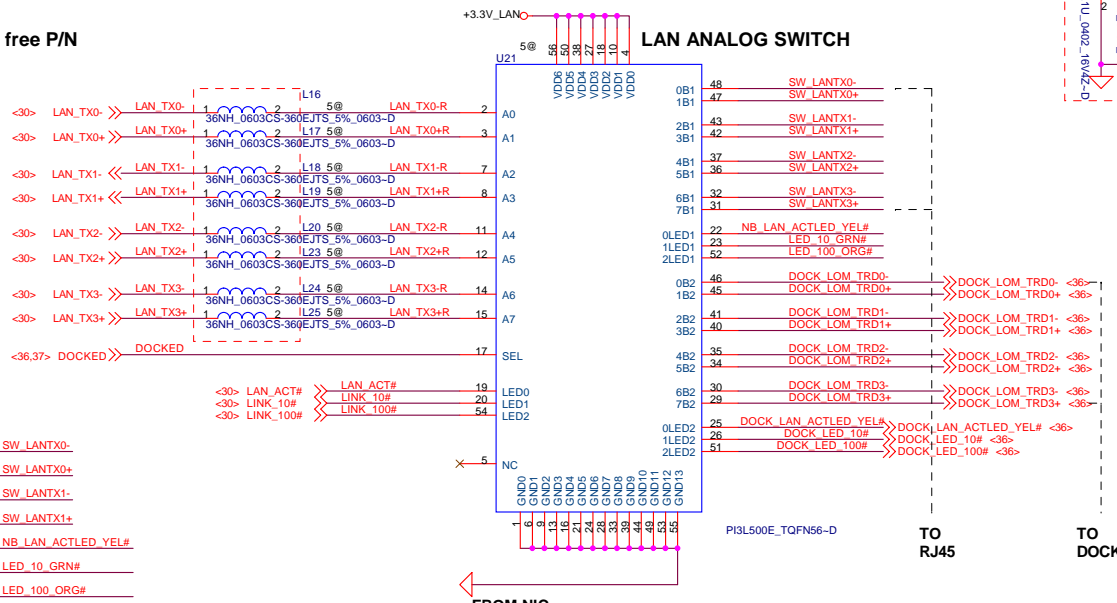


R359, R360, R364, R366 pop 49.9_1%
ohm resistor for 4401E LOM



TYCO_1368458-1 & Belfuse_L830-1J1C-47 / 4401E
TYCO_1368938-2 & Belfuse_L830-1J1C-43 / 5752

Apply lead free P/N



Place these caps as close
to the center tap pins
of the mag/connector.

FROM NIC
DOCKED 1: TO DOCK
0: TO RJ45

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PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

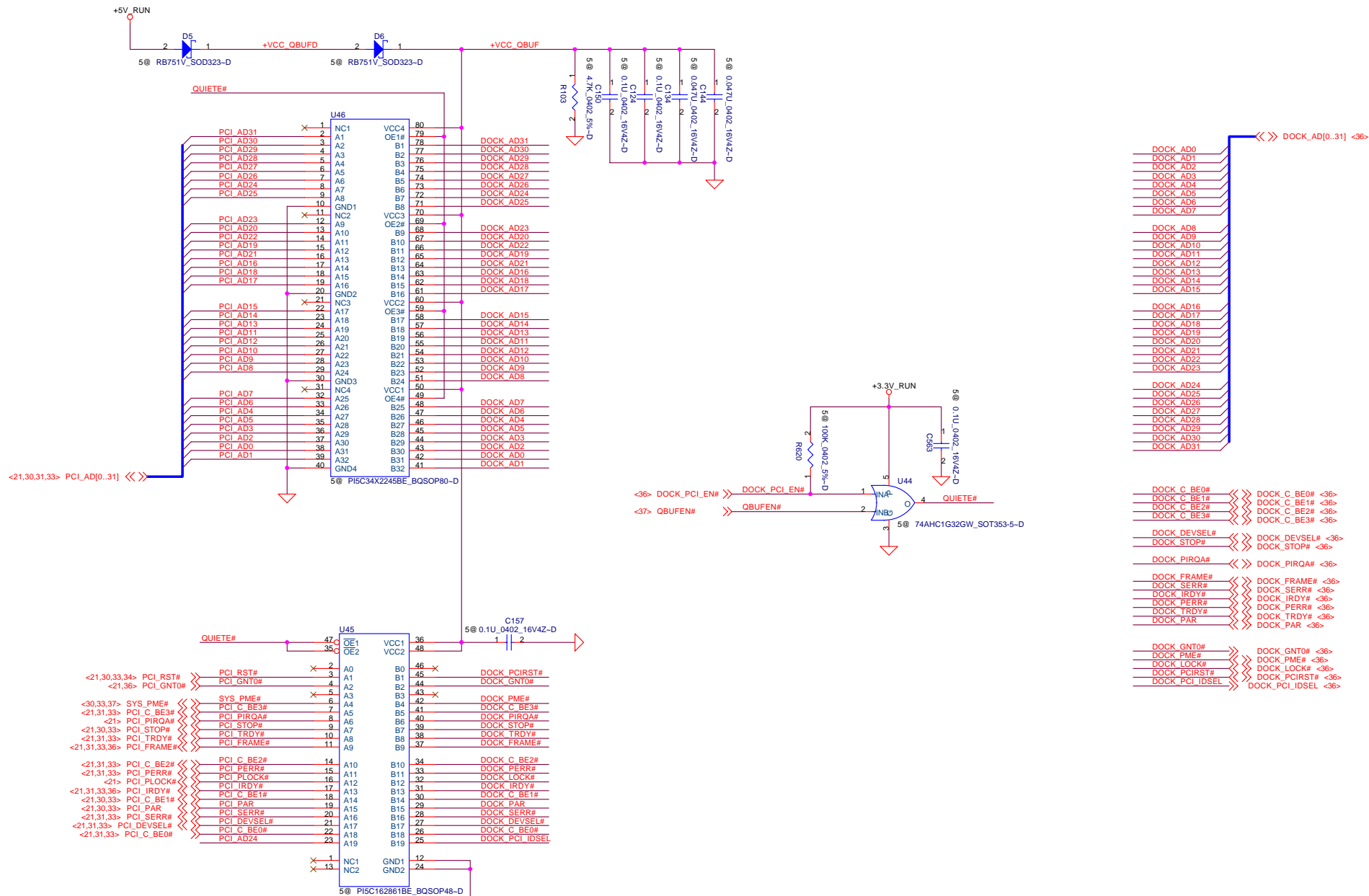
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Compal Electronics, Inc.

LAN Transfomer and RJ45

LA-2881P

Date: Tuesday, December 13, 2005 Sheet 32 of 62



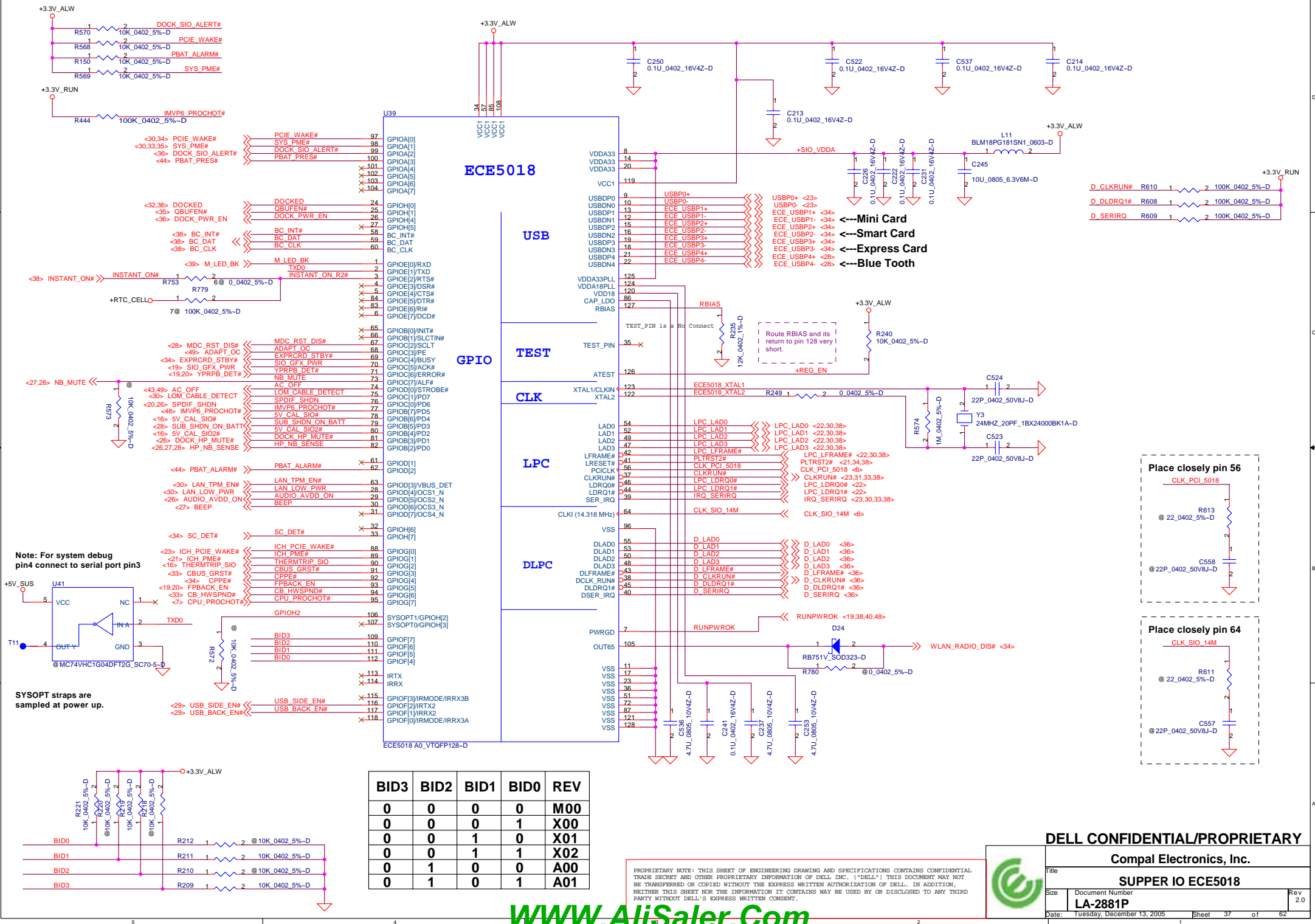
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Compal Electronics, Inc.

Title		
DOCKING BUFFER		
Size	Document Number	Rev
	LA-2881P	2.0
Date	Tuesday, December 13, 2005	Sheet 35 of 62

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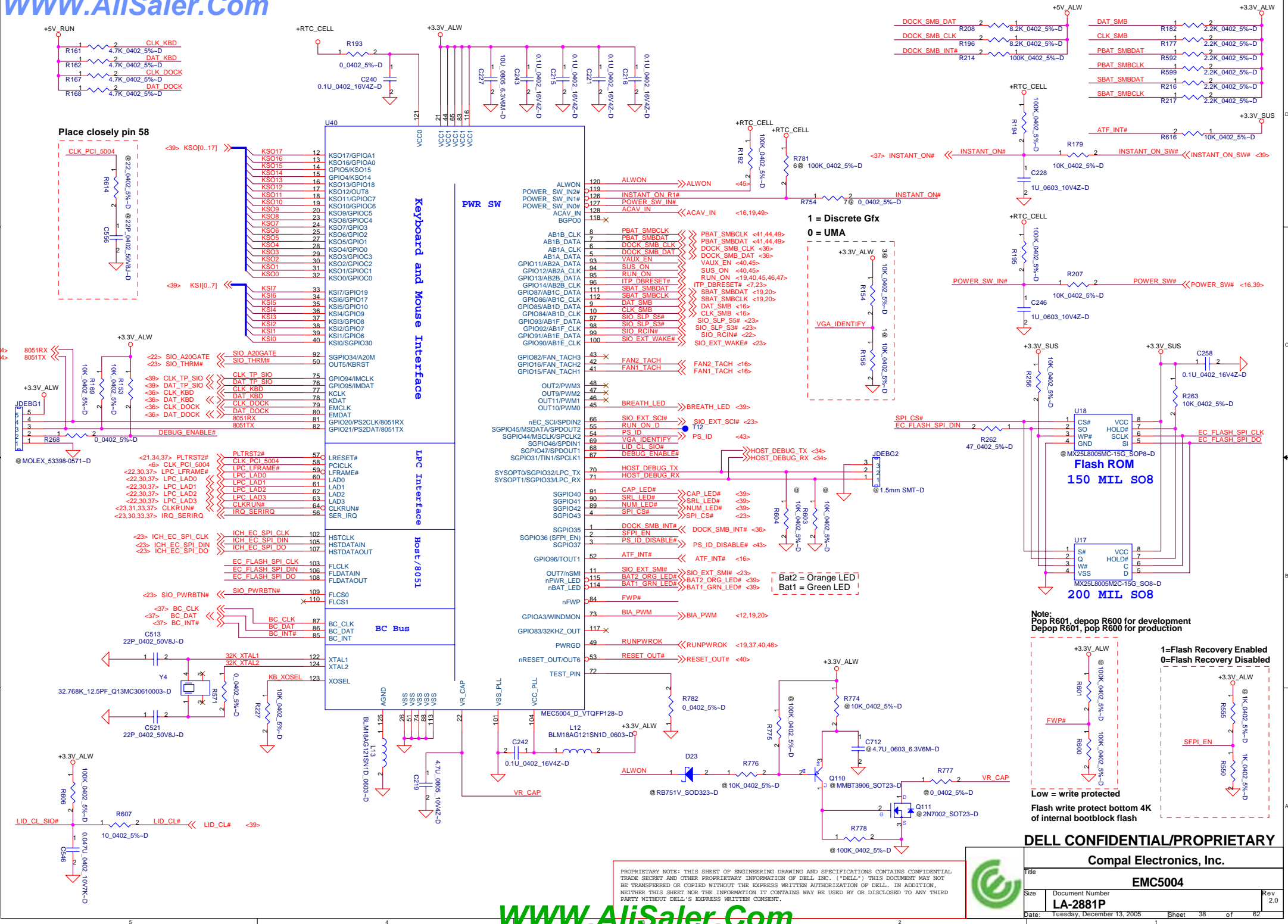


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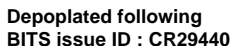
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Size Document Number
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13.7uA leakage current at S3

Maximum Rds on value for Q41, Q89 and Q90 should 15 mohm

+3.3V_SUS Source

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POWER CONTROL AND SEQUENCE

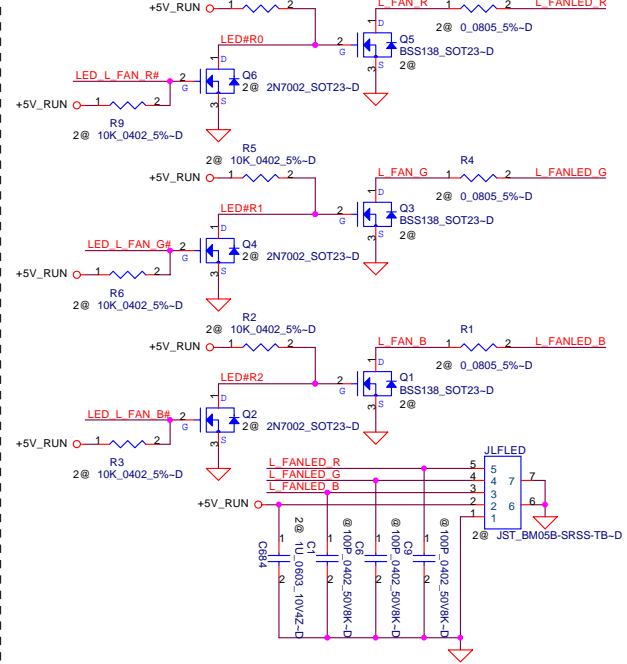
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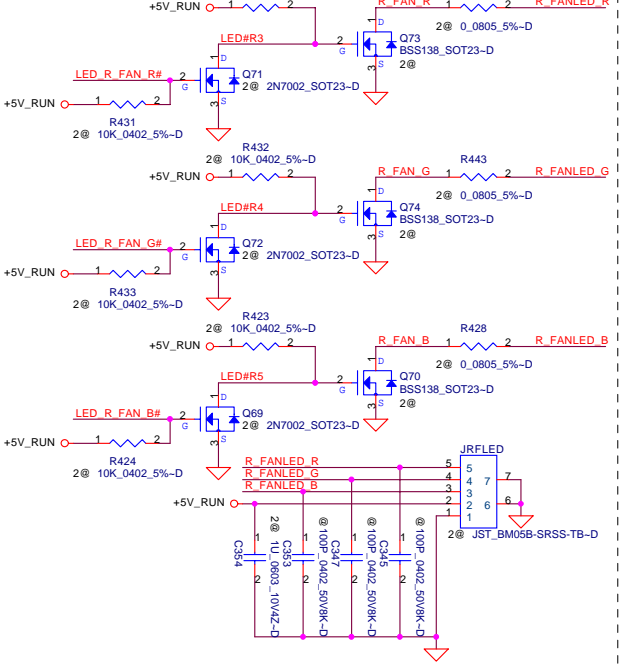
Rev
2.0

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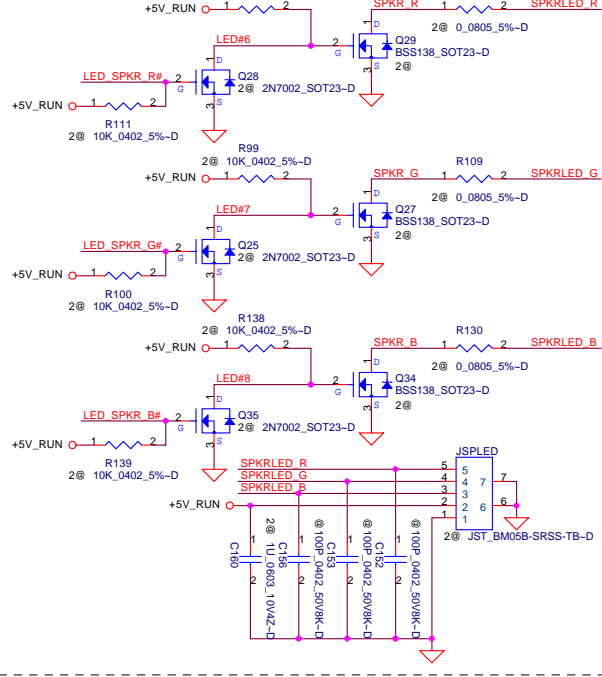
LEFT FAN



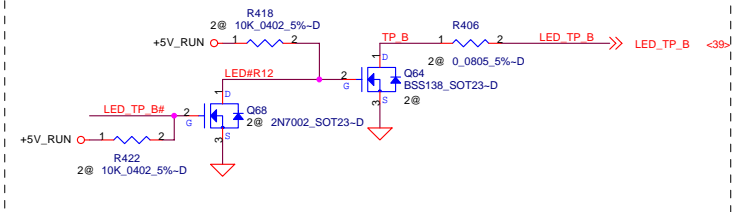
RIGHT FAN



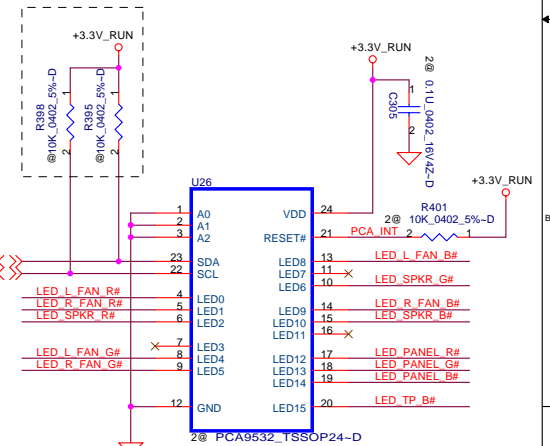
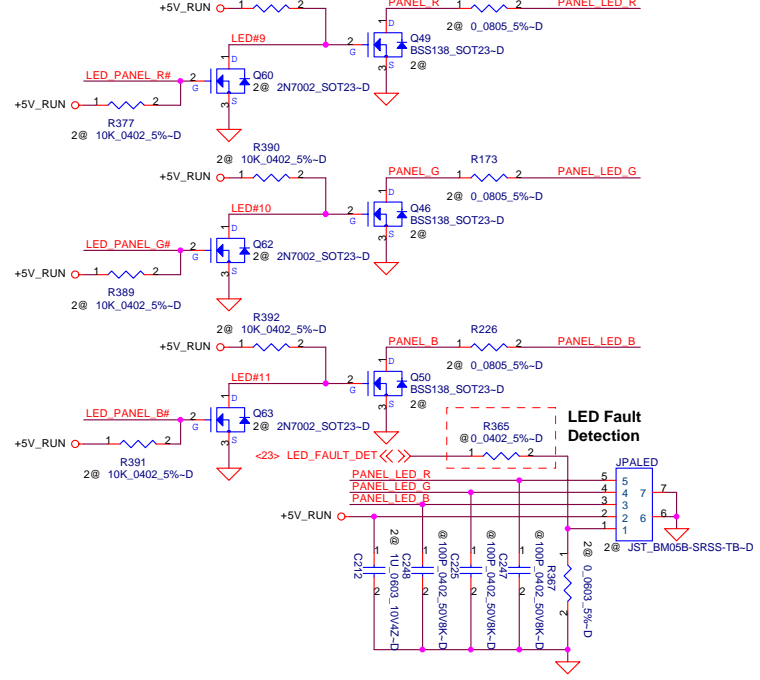
SPKR LED



TP LED



PANEL LED



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Title	Rikers LEDs for FAN/Speaker/Panel/TP		
Size	Document Number	Rev	
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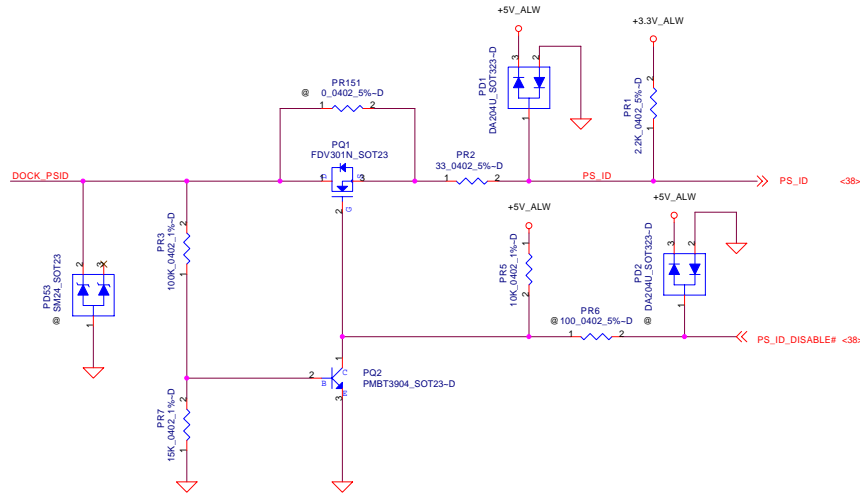


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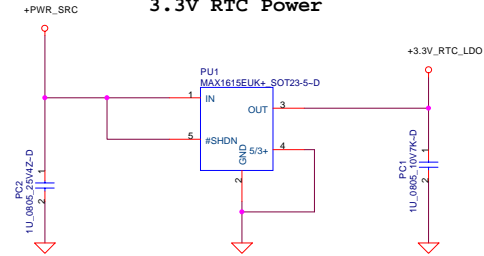
PAD and Standoff		
Size	Document Number	Rev

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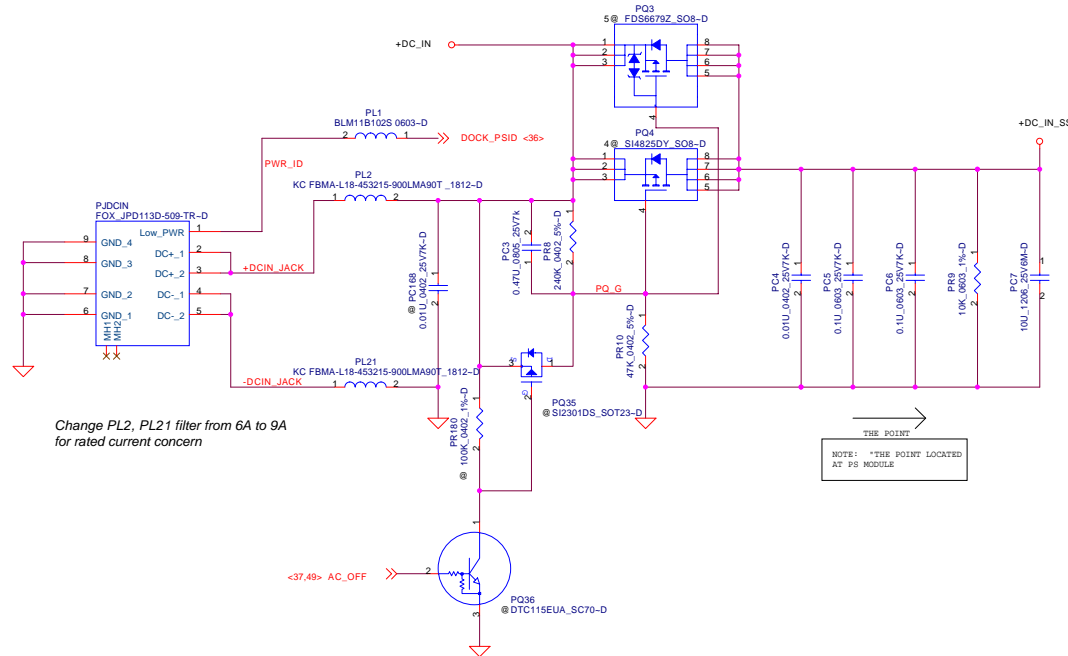
PS_ID Detector



3.3V RTC Power



+DC_IN Source

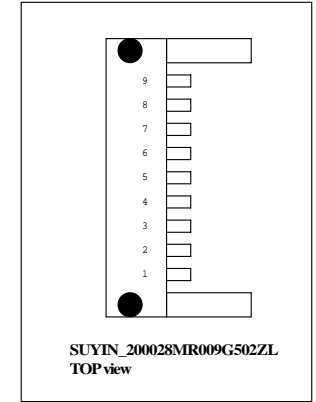
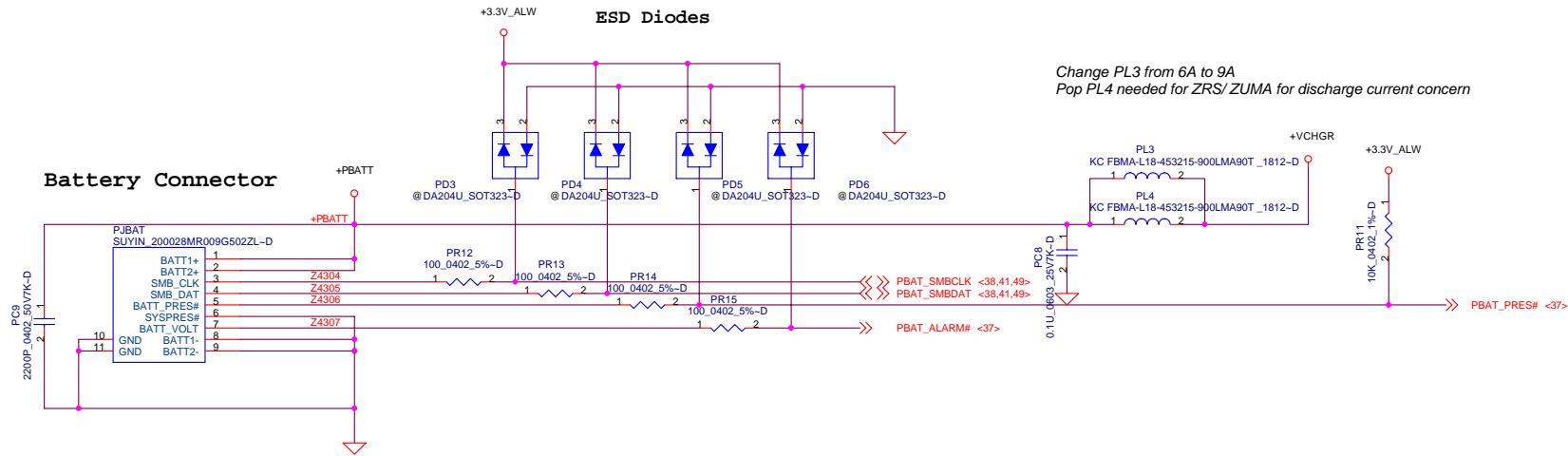


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+DCIN

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Battery Conn

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DC +3.3V/ +5V

3.3 Volt +/-5%
Typical current: 4.67A
Max current: 6.67A
Min OCP: 7.4A

5 Volt +/-5%
Typical current: 4A
Max current: 5.6A
Min OCP: 8.5A

Output Caps ESR
= 25mohms

Output Caps ESR
= 25mohms

Return to original design due to
SMSC issue already be fixed.

Leverage Sullivan

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+3.3V/+5V/+15V



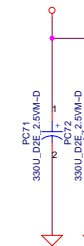
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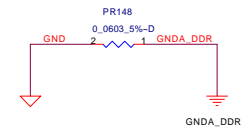
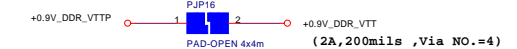
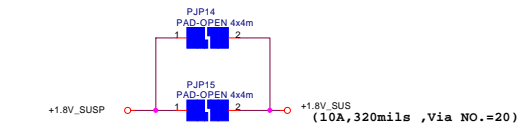
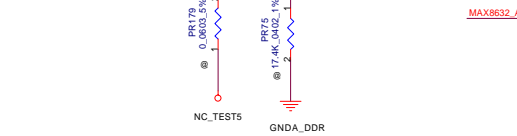
+1.8V_SUSP/ +0.9V_DDR_VTTP
DDR2 Termination

1.8 Volt +/-5%
Design Current: 7.3A
Maximum Current: 10.5A
OCF min: 10.5A

+1.8V_SUSP

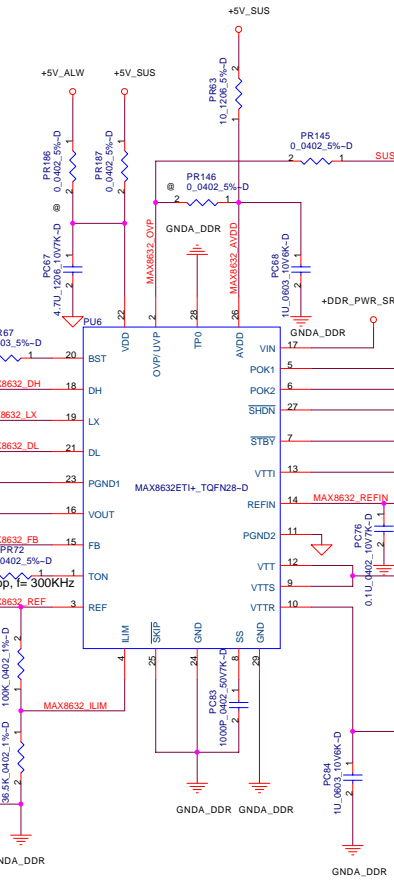
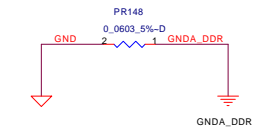


Output Caps ESR
= 15mohms/ each



Place these CAPS
close to FETs

L-S Rds-on (max)
=4.8m ohms



0.9 Volt +/-5%
Design current 1.05A for +0.9V_DDR_VTTP
Peak current 1.5A for +0.9V_DDR_VTTP

0.9 Volt
VTTR current limit: +-32mA typ

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DELL CONFIDENTIAL/PROPRIETARY			
Title +1.8VSUSP/ +0.9V_DDR_VT			
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	SIO	06/22/2005	Compal	BID change to X00.	Pop R549, depop R553.	X00
2	42	Rikers LED	06/22/2005	Dell	Reserved LCM and Backlight circuit and depop on Rikers.	Depop Q104~Q107, R913~R918, C910, C920, JLMLED and JKBLED.	X00
3	20	CRT	06/27/2005	Compal	Buffers are duplicated on the video card, so added by pass resistors on Discrete mode.	Added R967,R968,C923,C924	X00
4	20	CRT	06/27/2005	Compal	Connected HSYNC and VSYNC to docking connector from the output of U194 and U195.		X00
5	38	EMC5004	07/06/2005	Compal	Added a DIP switch for the Flash recovery disable/enable function at develop phase.	Added SW1 and pop R591. Added R622, R623 reserved for bypass SW1.	X00
6	37	ECE5018	07/06/2005	Compal	+3VRUN leakage at AC mode in S5	Change R533 pull up from +3.3V_SRC to +3.3V_RUN	X00
7	37	ECE5018	07/08/2005	Compal	Internal speaker no sound.	Pop R545	X00
8	07	CPU	07/11/2005	Dell	Updated ITP pullup resistor values as M07-discrete-A03 Ref. Sch.	Change R81~R86, R77, R196 value.	X00
9	07	CPU	07/11/2005	Dell	Updated H_PROCHOT# pullup resistor values as M07-discrete-A03 Ref. Sch.	Change R548 to 75 ohm.	X00
10	40	POWER SEQUENCE	07/11/2005	Dell	Updated Power Good circuit as M07-discrete-A03 Ref. Sch.	Added R617, R619, R620, R621, Q51, Q52, Q53, Q64.	X00
11	06	CLOCK GENERATOR	07/12/2005	Dell	Updated clock GEN. resistor values as COE X04 Ref. Sch.	Change R36,R37,R43,R45,R49,R919,R33,R35 value to 15 ohm.	X00
12	36	Docking Connector	07/12/2005	Dell	Update docking circuit as COE A03 ref. sch.	Made R899,R900,R901,R902 no stuff.	X00
13	16	Thermal sensor	07/12/2005	Dell	Change R701 so that C158 and C159 are between LDO_IN and R701.	Change R701 location.	X00
14	19 & 37	GFX CONN. ECE5018	07/12/2005	Dell	Follow COE graphic card A05 ref. sch.	Change the net name of pin1 of U5 to SIO_GFX_EN	X00
15	34	MINI card	07/12/2005	Dell	No filtering on +3.3V_LAN	Added C925	X00
16	07	CPU	07/12/2005	Dell	Per Intel checklist rev 1.3 and CRB rev 1.4	Added pull down R969 for TEST1	X00
17	40	POWER SEQUENCE	07/12/2005	Dell	Follow COE graphic card A05 ref. sch.	Added RUN_ENABLE off-page connection	X00
18	14	Calistoga-PWR	07/12/2005	Dell	Per Intel checklist rev 1.3 and CRB rev 1.4	Added C926 and C927.	X00
19	40	POWER SEQUENCE	07/13/2005	Dell	Follow COE UMA A07 and Core discrete A04 ref. sch.	Added R970~R975, C928, Q118 and U40C.	X00
20	16	Thermal sensor	07/13/2005	Dell	Follow COE UMA A07 and Core discrete A04 ref. sch.	Added 2.5V_RUN_PWRGD off-page connection on pin 31 of U4	X00
21	33	R5C832	07/13/2005	Dell	May potentially have leakage current into R5C832.	Added R976 and no stuff.	X00
22	26	CODEC	07/13/2005	Dell	Change GPIO0 control to HP_NB_SENSE, internal EQ will be controlled by codec jack sence.	Connected HP_NB_SENSE to pin 21 of U188, and added R977 no stuff.	X00
23	26 & 27	CODEC Amplifier	07/13/2005	Dell	Move PC BEEP circuit from CD inputs of codec to internal speaker amplifier.	C414 depop and change R381 value to 2.2K ohm.	X00
24	27	Amplifier	07/13/2005	Dell	Add place holders for 47pF caps on positive inputs of speaker amplifier. Change GPRS immunity caps to no stuff by default. Signal removed to allow BEEP while headphones plugged in.	Added C929,C930 no stuff. Depop C885,C886. Remove Q29.	X00

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	33	1394	07/13/2005	Dell	Reserved common mode chokes for EMI and added 0 ohm resistors to bypass 1394 signals for cost saving.	Added R978~R981 and L90, L91 depop.	X00
26	34	EXPRESS CARD	07/13/2005	Dell	Reserved common mode chokes for EMI and added 0 ohm resistors to bypass USB signals for cost saving.	Added R982, R983 and L92 depop.	X00
27	24	ICH7-M	07/14/2005	Dell	Follow COE ICH A03 ref. sch.	Depop C349, C350, C359.	X00
28	23	ICH7-M	07/14/2005	Dell	Follow COE ICH A03 ref. sch.	Change R711 from 8.2K no stuff to 10K stuff.	X00
29	38	EMC5004	07/14/2005	Dell	ITP_DBRESET# not on wake pin.	Swapped ITP_DBRESET# and RUN_ON_D.	X00
30	37	ECE5018	07/14/2005	Dell	SPDIF_SHDN at the codec is +5V.	Connected SPDIF_SHDN to pin 76 of U36.	X00
31	37	ECE5018	07/14/2005	Dell	Follow COE Latitude EC A02 ref. sch.	Added GPIOs AC_OFF and LOM_CABLE_DETECT.	X00
32	37	ECE5018	07/14/2005	Dell	Missing series resistor on Xtal.	Added R984.	X00
33	3	Index	07/14/2005	Compal	Update PCI table.		X00
34	16	Thermal sensor	07/14/2005	Dell	Change decoupling for VDD_5V	Swap location of C160 and C161.	X00
35	37	ECE5018	07/15/2005	Dell	Removed level shift circuit.	Delete R546, R547, Q42	X00
36	40	POWER SEQUENCE	07/15/2005	Dell	Add +2.5V_RUN bleed of ckt as UMA A07 schematic.	Added R988, Q121 and no stuff.	X00
37	39/41/42	TP LED	07/15/2005	Dell	Will use tri-color TP LED on Rikers.	Added R985,R986,R987,Q119,Q120. Remove LCM circuit and connected TP LED control signal. Connected the pin 1 of R645 to +5V_ALW and pin 1 of R644 to +15V_SUS.	X00
38	40	POWER CONTROL	07/15/2005	Dell	Follow COE UMA A07 ref. schematic.	R646,R647 no stuff and change R644 value to 100K.	X00
39	13	Calistoga	07/19/2005	Compal	Changed resistor package from 0402 to 0603 for Increasing VCCD_LVDS Power Rating.	Changed R168, R169, R182, R183.	X00
40	30/37	LOM/ECE5018	07/19/2005	Dell	5752M Hooks not in place. Need to connect Pin C04 (Energy Detect to pin 75 GPIOC1 of the champion chip)	Added R228 (5@)	X00
41	30	LOM	07/19/2005	Dell	LOM_LOW_PWR signal must be connected to 4401 Export# signal also.	Added R231 (4@)	X00
42	33	R5C832	07/19/2005	Dell	Rename +3V_PHY to +3VRUN_PHY per ref schematic.	Changed Net Name	X00
43	33	R5C832	07/19/2005	Dell	UDIO3, UDIO4, XDEN, MSEN pins can be pulled up to +3V_R5C832 through a single 10k resistor.	Deleted R487, R488, R489.	X00
44	33	R5C832	07/19/2005	Dell	Rename +XD_VCC to +3VRUN_XD per ref schematic	Changed Net Name	X00
45	33	R5C832	07/19/2005	Dell	Rename +VCC_5IN1 to +3VRUN_CARD per ref schematic	Changed Net Name	X00
46	33	R5C832	07/19/2005	Dell	150k-ohm pull-down to GND is needed on +VCC_5IN1 for media card detection per Ricoh. This is R21 on M07 ref schematic	Added R501	X00
47	7/37	CPU/ECE5018	07/20/2005	Dell	Rename H_PROCHOT# to CPU_PROCHOT# on page 7. Rename H_PROCHOT# to IMVP6_PROCHOT# on page 49, and route to ECE5018 pin 77. Add 100k ohm pull-up on IMPV6_PROCHOT# to +3.3V_RUN on page 37. Rename PROCHOT_SIO# (page 37) to CPU_PROCHOT# and route to cpu pin D21 (leave pull-up)	Added R60 (100K Pull Up).	X00

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
48	23	ICH7M	07/20/2005	Dell	SPI pullup location doesn't match DG (M07_ICH7_A04)	Moved R365 to left of R713	X00
49	23	ICH7M	07/20/2005	Dell	HDD_DET# not needed (M07_ICH7_A04)	Renamed GPIO12 to RSVD_HDD_DET#	X00
50	23	ICH7M	07/20/2005	Dell	Change SATAGP[0-3] to pullup as M07_ICH7_A04 CoE Ref Schematic	Deleted R345, R961~R966.	X00
51	33	R5C832	07/20/2005	Dell	Power switch follows up the recommended switch in ref schematic. Use the AAT4250	U26 changed to AAT4250	X00
52	36	DOCK	07/20/2005	Dell	DOCK can't be enabled	Changed DOCK pin 238 connection to ICH7M PCI_REQ0# directly from PCI Buffer (U31).	X00
53	26	CODEC	07/20/2005	Dell	Follow COE AUDIO A03 ref.sch.	Remove C414.	X00
54	6	CLOCK	07/21/2005	Dell	Item Id: CR03833 Title: Change 0.1uF cap to 10uF cap	Changed C7	X00
55	37	ECE5018	07/21/2005	Dell	Need to move the NB_MUTE GPIO to C7 (pin 73). The original GPIO CANNOT be programmed to drive.(SMSC Silicon issue)	Changed connection	X00
56	23	ICH7M	07/21/2005	Dell	Per the ICH reference schematic A04, need to move the pull-up on ICH_EC_SPI_DO to the other side of R713.	R365 has been moved to the left of R713	X00
57	37	ECE5018	07/21/2005	Dell	Media button LED always ON issue.	Connected M_LED_BK to pin 1 of U36.	X00
58	22	ICH7M	07/21/2005	Dell	ICH_INTVRMEN is missing the NP 0 ohm pulldown at pin 2 of R323.	Add R989 no stuff.	X00
59	23	ICH7M	07/21/2005	Dell	LAMP_STAT# pullup resistor should be tied to +3V_SUS.	R711 tied to +3V_SUS.	X00
60	23	ICH7M	07/21/2005	Dell	Per ICH M07 Ref Schematics Rev A04.	Changed R358 value to 680 ohms.	X00
61	23	ICH7M	07/21/2005	Dell	SIO_EXT_WAKE needs a 0 ohm series resistor at the ICH Pin AC21.	Add R990.	X00
62	24	ICH7M	07/21/2005	Dell	Per ICH M07 Ref Schematics Rev A04.	Add R991,R992 and pop C534,C362.	X00
63	25	CD-ROM	07/21/2005	Dell	Per ICH M07 Ref Schematics Rev A04	Changed R375 value to 510 ohms and JMOD name to JODD. Change the JMOD pin 37 name to IDE_LED#	X00
64	37	ECE5018	07/22/2005	Dell	SYS_PME# is pulled up to 3VRUN. It is pulled up to 3VALW in the M07 EC Ref Schematics Rev. A02	Changed R533 pulled up[to +3.3V_ALW.	X00
65	37	ECE5018	07/22/2005	Dell	SIO_GFX_EN is named differently from the Ref Schematics. It is named SIO_GFX_PWR in the M07 EC Ref Schematics Rev. A02	Changed Netname.	X00
66	33	1394	07/22/2005	Compal	For 1394 TPB0+ and TPB0- layout routing smooth.	Swap L91, R980 and R981.	X00
67	38	EMC5004	07/22/2005	Compal	EC debug requirement for design phase, will be removed after MP.	Pop JDEBG1 connector.	X00
68	16	Thermal sensor	07/23/2005	Dell	Follow GuardianII X03 reference schematics.	Add a note to U4 that states "Solder thermal pad to plane. Add 9 ground vias to pad."	X00
69	13	Calistoga	07/23/2005	Dell	Per the UMA reference schematic A07.	Add note to place C100/C99/C96 close to pin AB1/D2/A6.	X00
70	24	ICH7M	07/24/2005	Dell	C341 should be 330uF. It is currently 220uF. Per ICH M07 Ref Schematics Rev A04. (Item Id: DF04040)	Change C341 value to 330uF.	X00
71	10	Calistoga	07/24/2005	Dell	Need to POP R140 to enable testing C4 Latency.(Item Id: DF04038)	Populated R140.	X00
72	All Pages	N/A	08/02/2005	Compal	Renamed all parts Reference	All Parts but Connector	X01

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
73	6/31	CLOCK/LOM	08/02/2005	Dell	Avoid running clk_pci_lan throun RN8 as Layout Issues list request.	Changed R206 as 4@. Changed CLK_PCI_LAN connection.	X01
74	37	SIO	08/02/2005	Dell	Changed BID	Changed R221, R211 as @. Changed R220, R212 as pop.	X01
75	6	CLOCK	08/03/2005	Dell	Add 0.1uF cap to +CK_VDD_MAIN so that each VDD pin has a cap (CoE CLOCK Ref Sch X05)	Added C699.	X01
76	17/18	Memory	08/03/2005	Dell	Connected pin 50 of DIMMA to pin 50 of DIMMB and named net PM_EXTTTS#0_R. Remove No Stuff attribute from R118(Old Ref R213).Delete R118(Old Ref R218), 0 ohm, and connection to PM_EXTTTS#1. (CoE Memory Ref X03)	Deleted R117(Old Ref R218). Populated R118(Old Ref R213)	X01
77	16	Guardian II	08/03/2005	Dell	Removed pull-up at LDO_POK. Pullup is on power sequence.(CoE Guardian II Ref X04)	Deleted R47(Old Ref R227)	X01
78	16	Guardian II	08/03/2005	Dell	Add voltage margin circuit(CoE Guardian II Ref X04)	Added R737	X01
79	16	Guardian II	08/03/2005	Dell	Add additional thermistor circuit(CoE Guardian II Ref X04)	Added R738~R743. C700, C701, Q102, Q103.	X01
80	21	ICH7M	08/03/2005	Dell	Component not required.(CoE Latitude EC Ref A03)	Unpoped C46 (Old ref C892)	X01
81	38	KBC	08/03/2005	Dell	ATF_INT# pullup should be +3.3V_SUS(CoE Latitude EC Ref A03)	Change R616(Old ref R570) pullup to +3.3V_SUS.	X01
82	10	GMCH	08/03/2005	Dell	Remove PM_EXTS#1 connection options to the SODIMM. Use this to implement C4E implementaion Only(CoE UMA Ref A08)	Deleted R701(Old ref R139)	X01
83	20	LVDS/ TV_OUT/ CRT	08/04/2005	Dell	Item Id: CR03751 Title: Add note to place 0-ohm resistors close to buffer	Added Note.	X01
84	4	Power Rails	08/08/2005	Compal	Update Power Rails	Added +3V_ALW Block	X01
85	4	SMBUS	08/08/2005	Compal	Update SMBUS Pull-Up Power Rail	Modified +3V_ALW instead of +3.3V_SRC	X01
86	77	Yonah	08/08/2005	Compal	Update ITP port resistor pop option.	Depopulated R735 as CoE Ref Schematic.	X01
87	7	Yonah	08/08/2005	Dell	Change 22uF Caps from X5R to X6S	Changed C4, C5, C7, C8, C10~C13, C15~C18, C662~C664, C658, C668~C675, C677, C678, C681, C682, C686~C689	X01
88	33	R5C832	08/12/2005	Dell	Updated the electrical countermeasure circuit for the MS Duo Adapter short issue (CoE 1394 Ref A06)	Added D22, R117. Changed Q76 to P MOSFET.	X01
89	33	R5C832	08/12/2005	Dell	Changed part for the common mode choke since the proper impedance for 1394 is 110 to 200-ohms(CoE 1394 Ref A06)	Changed L90, L91 to DLW21N121SQ2 as nopop.	X01
90	26/37	AUDIO/SIO	08/12/2005	Dell	Add GPIO to control internal speaker mute when docked and HP plugged in.	Added DOCK_HP_MUTE# signal and 100K pullup (R701).	X01
91	26/27/28	AUDIO/ Amplifier	08/12/2005	Dell	Add EAPD signal back in for future power savings opportunities. Default NP. Added EAPD to GPIO3, also 2N7002 control to speaker and sub shutdown pins. A04	Added Q104, Q105 as Nopop.	X01
92	12	GMCH	08/12/2005	Dell	NO STUFF Resistor for the CFG11 (CoE Ref Sch. 945PM_GM_M07_A00)	Nopop R678	X01
93	19/20/40	GMCH/Power	08/12/2005	Dell	Changed net name INV_PWRSRC to GFX_PWR_SRC (CoE CRT_LVDS_SVIDEO M07_A00)	Changed Netname +G_PWR_SRC to +GFX_PWR_SRC	X01
94	20	LVDS	08/12/2005	Dell	Adding SVIDEO with SPDIF option Note (CoE CRT_LVDS_SVIDEO M07_A00)	Added Note	X01
95	40	Power	08/12/2005	Dell	Added Power Down Ckt (CoE M07 System POWER SEQUENCE A01)	Changed R170, R558 to 20K as Populated	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
96	40	Power	08/12/2005	Dell	Patch for the Yonah ICCP issue (CoE M07 System POWER SEQUENCE A01)	Changed R476, R477, R483, R484 to 0 ohm as Populated. Added R744 as populated.	X01
97	20	LVDS	08/15/2005	Dell	Support M07 inverter on ZUMA. Duplicate pull down on PANEL_BKEN.	Depop D7, U10 and pop R152, R133.	X01
98	10/12	Calistoga	08/16/2005	Dell	Follow CoE Core/945PM_GM M07_A01 schematic.	Adding notes for discrete implementation and depop R683.	X01
99	29	USB	08/16/2005	Dell	10uF caps at USB switches are optional.	Depop C554, C217 and C680.	X01
100	23	ICH	08/16/2005	Dell	SIO_EXT_SCI and SIO_EXT_SMI# causing leakage to +3.3V_RUN on S3 mode.	Changed pull up power rail from +3.3V_RUN to +3.3V_SUS.	X01
101	16	Thermal sensor	08/16/2005	Dell	Follow D05, ALWON is driven high and pull up is on VR reference design.	Depop R702.	X01
102	37	ECE5018	08/16/2005	Dell	Add new GPIOs(CoE Latitude EC ref A04)	Added HP_NB_SENSE back to pin 82 of U36.	X01
103	28	MDC	08/20/2005	Dell	Change disable fet to lower Vgs. Corrects circuit issues(CoE M07_MDC_A03)	Q61 changed to BSS138.	X01
104	40	Power Sequence	08/20/2005	Dell	Adding Clamp Ckt for 1.8VSUS, 3.3VUS and 5VSUS	Added R47, R745, R746, Q106~Q108. Deleted R171, R188. Changed bleed resistors from 22 to 30 ohm.	X01
105	10	GMCH	08/20/2005	Dell	Delete 40.2ohm pull down resistors for M_OCDCOMP0/1 and replace them with Test Points. Per Intel DG 1.0(CoE 945_a02)	Deleted R663, R682. Added T24, T25.	X01
106	10	GMCH	08/20/2005	Dell	Add 0.1 uf (402) for the DDR VREF at Calistoga for better noise immunity (CoE 945_a02)	Added C702 and pop C146.	X01
107	10	GMCH	08/20/2005	Dell	Remove H_DPRSTP# and H_DPSLP#. Previously they No Stuff. Per Intel (CoE yonah_m07_a01)	Deleted R720, R724.	X01
108	37	ECE5018	08/20/2005	Dell	NB_MUTE Pull down Resistor Reserved as Nopop as CoE Ref Sch (EC_A03).	Depoped R573.	X01
109	2	Block Diagram	08/20/2005	Dell	Update LOM 4401E from PCIe to PCI Bus		X01
110	33/41/42	4-in-1/LED	08/22/2005	Compal	Update Lead Free Layout Library.	Updated U29, Q76, Q5, Q3, Q1, Q73, Q74, Q70, Q29, Q27, Q34, Q49, Q46, Q50, Q36, Q12, Q64, Q66.	X01
111	23/29/37	USB	08/23/2005	Dell	Swapped the ICH USB port0 and port5.		X01
112	23	ICH	08/23/2005	Compal	LAMP_STAT# causing leakage to +3.3V_RUN and +5V_RUN on S3 mode.	Depoped R554.	X01
113	38	EMC5004	08/24/2005	Dell	FWP# should be pulled high for development and pulled down for production.	Change pop option for FWP# for development and production.	X01
114	23	ICH	08/24/2005	Dell	BITS item ID: CR05958 Change value of SPI pull-ups.	Change R537, R538, R542 value from 1K to 10K ohms.	X01
115	33	4-in-1	08/24/2005	Dell	Adding bypass MS Duo short circuits in the event that the connector would be corrected	Added R747~R750 as no pop (@).	X01
116	13	GMCH	08/24/2005	Dell	TeamTrack: BITS Item Id: CR06800 Title: Calistoga Filter Issues page 13	Added R751, R752, C703, C704.	X01
117	10/40	GMCH/Power Sequence	08/24/2005	Dell	TeamTrack: BITS Item Id: DF06790 Title: Power Sequence Circuit, and C4-E and SPDIF Issues	Populated R302, R307, Q54, Q53, R306, R301, Q56, Q57, R683. Depoped R623.	X01
118	20	LVDS	08/24/2005	Dell	TeamTrack: Item Id: DF06789 Title: BIA_PWM for UMA need to add AND GATE	Added U49, C705, C706.	X01
119	22	ICH7M	08/24/2005	Dell	TeamTrack: Item Id: CR05951 Title: Move C535 to other side of R584	Moved C535.	X01
120	23	ICH7M	08/24/2005	Dell	TeamTrack: Item Id: CR05955 Title: Depop pull-up on SIO_THRM#	Depoped R598.	X01

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121	23/30/34	ICH7M/PCIE	08/24/2005	Dell	BITS CR05959: Rename PCI-E nets	Renamed PCI-E Nets.	X01
122	22/25	ICH7M/SATA	08/24/2005	Dell	BITS CR05950: Rename SATA Rx / Tx lanes	Renamed SATA Rx/Tx Nets.	X01
123	13	GMCH	08/26/2005	Dell	TeamTrack: BITS Item Id: CR06800 Title: Calistoga Filter Issues page 13	Added C707, C708. Deleted R665, R679, R671, R675.	X01
124	13	GMCH	08/26/2005	Dell	It is part of the Intel Filter ckt, for now you could place 0 ohm 805 package. The key is to reserve a placement for this component, in case you got an issue with your platform that related to this power rail noise. "	Changed Value of R751, R752 to 0 ohm.	X01
125	13	GMCH	08/26/2005	Dell	Updated the schematic notes for the MS-Duo Adapter Countermeasure Circuit.		X01
126	4	Power Rails	08/26/2005	Compal	Added +2.5V_RUN Rail Diagram		X01
127	7	CPU	08/26/2005	Dell	Per Intel DG rev 1.0 and M07 Ref Schematic.	Chnage R714 to 1K, R723 to 51ohm.	X01
128	39	Touch Pad	08/26/2005	Compal	For TP cable is compatible with Sullivan.	Swapped JTP pin1 and pin2.	X01
129	12	Calistoga	08/29/2005	Dell	PANEL_BKEN has twice pull down.	Removed R631.	X01
130	5	SMBus Topology	08/29/2005	Compal	Update SMBus Diagram.		X01
131	37/38	ECE5018 EMC5004	08/29/2005	Dell	Media direct button don't power on the system for Suva.	Add R754 for Zanzibar/ZUMA/Rikers only and R753 for Suva only.	X01
132	1	Cover page	08/29/2005	Dell	Add 6@ for Suva used only and 7@ for Zanzibar/ZUMA/Rikers used only.		X01
133	20	SPDIF	08/30/2005	Dell	Remove the transformer for SPDIF ckt.	Removed L29.	X01
134	20	CRT	08/30/2005	Dell	Added 39 ohm series resistors at HSYNC and VSYNC after the Buffer.	Added R755 and R756.	X01
135	20/43	TV_OUT	08/30/2005	Dell	Modified TV OUT filters for resolution support.	Added C709-C711 no stuff. C414,C417,C422,C413,C416,C421 pop 47P for discrete and 82P for UMA.	X01
136	16	Guardian II	08/31/2005	Dell	BITS CR20056: This is to address a D05 acoustic noise issue on the 5V Run rail.	Populated C410.	X01
137	30	LOM	08/31/2005	Dell	BITS CR20058: The comms teams recommedns that R507 and R522 be de-populated for all configurations.	Depopulated R507, R522.	X01
138	30	LOM	08/31/2005	Dell	BITS CR07184 and CR07190 Include support for ST-Micro Flash M45PE20 for the 5752 LOM	Added U50 and depop U24, R505. Added R757 nopop and pop R407, R509 for Rikers/Suva.	X01
139	34/38	MINI card EMC5004	09/02/2005	Dell	Debug Signals Routed to WLAN mCard connector.	Route HOST_DEBUG_TX/HOST_DEBUG_TX/8051TX/8051RX/ to JMINI pin16/17/19/42.	X01
140	12/20	Calistoga LVDS CONN	09/02/2005	Dell	Updated backlight control circuit.	Moved U49 and C705 to page 12. Pop R152 for UMA only.	X01
141	16	Guardian II	09/02/2005	Dell	Resistors package change for temperature/voltage margining test.	Change R737 and R703 from 0402 to 0603.	X01
142	39	LED	09/02/2005	Dell	BITS: CR03757 Updated bluetooth control circuit.	Added Q109.	X01
143	33	R5C832	09/05/2005	Dell	BITS DF20288: CoE5 Design review feedback from Arin Lin.	Change R487 value from 10K to 100K.	X01
144	30/43	LOM	09/05/2005	Dell	BITS CR20884:Based on IEEE testing, need to update RDAC value. This is ONLY for Zanzibar/Zuma using 4401E LOM.	Change R515 value from 1.27K 1% ohm to 1.24K 1% ohm. This change is for Zanzibar/ZUMA 4401E LOM only.	X01

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145	6/30/33	CLOCK/LOM /R5C832	09/06/2005	Compal	Crystal circuit evaluation.	Change C313,C314 value to 22pF and R199,R486 value to 220 ohm. R410 pop 750 ohm for 4401E, 470 ohm for 5752.	X01
146	5/38	SMBUS	09/07/2005	Compal	Fine tune SMBus pull-up resistors value.	Change R177/R182/R216/R217/R592/R599 value to 2.2K.	X01
147	43	Config.table	09/09/2005	Compal	4401E don't support TPM function.	Nopop R612 on ZUMA and Zanzibar.	X01
148	20/43	TV_OUT/CRT	09/13/2005	Dell	TV out filter circuit and termination changes for graphics.	Change R497,R503,R504,R17,R22,R26 value to 150 ohm. Change R755 and R756 from 39 ohm to 33 ohm.	X01
149	40	Power control	09/16/2005	Dell	Poplated +1.8V_SUS clamp circuit.	Pop R47 and Q106.	X01
150	37	ECE5018	09/23/2005	Dell	Board ID change.	Pop R221, depop R212.	X02
151	3/23/28/36	USB	09/29/2005	Dell	Added 0 ohm pop option for BT port	Useing ICH7-M port 7 for BT on Zanzibar/ZUMA. Added R758~R765.	X02
152	3/23/34/37	USB	10/11/2005	Dell	Added 0 ohm pop option for express card.	Useing ICH7-M port 0 for express card on Zanzibar/ZUMA. Added R766~R773.	X02
153	38	EMC5004	10/14/2005	Compal	Dip switch and JDEBG1connector are for development debug only, will remove for MP.	Remove SW1, R551, R552 and depop R555. Depop JDEBG1.	X02
154	37	ECE5018	10/14/2005	Compal	We can read system debug code from JDEBG2, so depop serial port inverter for cost saving.	Depop U41.	X02
155	39/41	Rikers LED	10/15/2005	Compal	Backlite Keyboard will not be supported and TP will only support single color LED on Rikers.	Remove page 42 and update intersheet references.	X02
156	38	EMC5004	10/15/2005	Dell	BITS item ID: CR29479 The MEC5004 boot block needs to be write protected.	Pop R600 and depop R601.	X02
157	20	CRT	10/15/2005	Dell	BITS item ID CR29469 : Per the VESA requitrement,change the VCC CRT diode to RB500 rated at Io = 100 mA Max.	Change D17 to RB500.	X02
158	40	Power sequence	10/15/2005	Dell	BITS item ID: CR29440 These are causing backdrive issue.	Deopulated R302, R307, Q54, Q53, R306, R301, Q56,Q57.	X02
159	13	Calistoga	10/15/2005	Dell	BITS item ID: CR29472 R751,R752 are not needed, replace these resistors by copper	Remove R751, R752.	X02
160	33	R5C832	10/15/2005	Dell	BITS item ID: DF20275 Follow Ricoh and M07 ref. schematic.	Remove R483.	X02
161	13	Calistoga	10/15/2005	Dell	Follow COE ref. sch. 945PM_GM_PM_M07_A04	Added notes for 3GPLL and 1.5V PCI-E power rails.	X02
162	34	Minicard	10/15/2005	Dell	Follow COE ref. sch. M07_minicard_A06 to remove resistors on COEX1_BT_ACTIVE and COEX2_WLAN_ACTIVE.	Removed R409 and R411.	X02
163	23	ICH7-M	10/15/2005	Dell	Follow COE ref. sch. ICH7_A06.	Moved LAMP_STAT# pull up resistor from +3.3V_SUS to +3.3V_RUN and pop R554.	X02
164	30	LOM	10/15/2005	Compal	Per broadcom ref. schematic.	Change Q59 from BCP69 to MBT352000MT1G.	X02
165	38	EMC5004	10/17/2005	Dell	Added a work around proposed by SMSC for the flash corruption issue.	Added D23,Q110,Q111,C712,R774~R778.	X02
166	37/38	EMC5004 ECE5018	10/18/2005	Dell	Added pull up resistors to +RTC_CELL on INSTANT_ON_R1# and INSTANT_ON_R2# for Rikers/Suva.	Added R779, R781.	X02
167	37	ECE5018	10/18/2005	Dell	Fixed a potential backdrive issue on the WLAN_RADIO_DIS# signal when we start doing Wake on WLAN.	Added D24 and R780 depoplated.	X02
168	38	EMC5004	10/18/2005	Dell	SMSC work around proposed for the flash corruption issue.	Added R782 connected TEST_PIN to GND.Change C219 value to 22uF and 0805 package for REV C parts.	X02
169	32	LAN Transfomer	10/19/2005	Dell	BITS DF06679:IEEE Return loss failures on Gig and 100 with Transpower DDOCK,these changes are just for Rikers/Suva only	Change R359,R360,R364,R366,R371,R374,R375,R382 to 48.7 1% ohm and L16~L20,L23~L25 to 36nH for Rikers/Suva only.	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
170	40	Power sequence	10/19/2005	Dell	5V_3V_RUN_PWRGD ckt values update to minimize the leakage current.	Change R302/R307 to 200K ohm, R301/R306 to 4.7K ohm.	X02
171	23	ICH	10/20/2005	Dell	Added 0.1uF cap as a short-term solution for IMVP_PWRGD glitch issue.	Added C713.	X02
172	19	DVI	10/20/2005	Dell	Reserved a 0805 pad for DVI safety issue.	Added R783.	X02
173	20	CRT	10/21/2005	Dell	Poplated CRT HSYNC and VSYNC buffer on discrete mode.	Change pop options on U4,U5,C653,C656,R41,R42,R38,R755,R756,R713,R707.	X02
174	3/23/28/34	USB	10/24/2005	Dell	Using the same USB mapping for Zuma,Zanzibar,Riker,and Suva	Update USB pop options.	X02
175	16	Thermal	10/26/2005	Dell	Follow COE M07_GUARDIANII_X05 ref. schematic.	Change R489,R490 to 120K and R488 to 78.7K 1%. Change C400,C694 to 22U and C412 to 0.22U.	X02
176	16	Thermal	10/28/2005	Dell	BITS item ID: CR20057 Change layout note for VCP thermistors	Updated Note.	X02
177	33	5-in1	10/28/2005	Dell	BITS item ID: DF20280 Layout for pins FIL0/REXT/VREF -- the ref designators need to be updated	Updated Note.	X02
178	27	Amplifier	11/01/2005	Dell	Set gain of TPA60017A2 to 21.6dB	Populate R449 and depop R453.	X02
179	28	Subwoofer	11/01/2005	Dell	Set gain of MAX9713 to 22 dB.	Populate R693 and depop R698.	X02
180	27/28	AUDIO	11/01/2005	Dell	Audio filter fine tune.	Change R685 to 0 ohm and C369, C343 from 0.015uF to 0.012uF. Depop C632 and change C383,C384 to 1U_10V_X5R. Change C620 from 0.056uF to 0.033uF.	X02
181	38	EMC5004	11/11/2005	Dell	Depop SMSC work around proposed on EMC5004 revision D chip	Depop R774~R778, C712, Q110, Q111 and D23. Change C219 from 22uF to 4.7uF	X02
182	37	ECE5018	11/12/2005	Dell	Board ID change to A00.	Depop R221, R220, R210. Pop R211, R212, R219.	A00
183	19	DVI	11/12/2005	Dell	To fix the overloading test failed issue on DVI port.	Change 0 ohm(R783) to RB500V(D25).	A00
184	23	ICH	11/12/2005	Dell	Follow COE ref. schematic ICH7_A07. HDDC_EN# and MODC_EN# floats at initial power up. Follow COE ref. schematic system power sequence_A05.	Added R783 and R784.	A00
185	40	POWER SEQUENCE	11/12/2005	Dell	Added +3.3V_RUN delay RC CKT to fix IMVP_PWRGD glitch issue Added diode bleed off for +3.3V_RUN GFX power down sequence adjustment.	Added R785 and D26. Change C81 from 0.01U to 4700P and C85 from 0.022U to 470P.	A00
186	40	POWER SEQUENCE	11/12/2005	Compal	Added clamp ckt for +5V_RUN.	Added R786 and Q112 but no stuff.	A00
187	16	Thermal	11/22/2005	Dell	BITS item ID: CR20057 Change layout note for VCP thermistors	Updated Note.	A00
188	23	ICH	11/22/2005	Dell	BITS item ID: CR05952 Change schematic notes on page 23.	Updated Note.	A00
189	26/27	AUDIO	11/22/2005	Dell	M07 cap change recommendations for audio.	Change C390,C395,C396,C362,C381,C382,C379 from Y5V to X5R and C363,C374,C380 from Y5V to X7R.	A00
190	39	LED	11/22/2005	Dell	Follow COE ref. schematic bluetooth_A06.	Change Q30 from PMBT3904 to BSS138.	A00
191	23/28/34	USB	11/24/2005	Dell	Since BIOS can fix bluetooth and express card issue on ST build. Remove 0 ohm pop options resistors for cost saving.	Remove R758~R773.	A00
192	28	Subwoofer	11/24/2005	Dell	Improveing the "BO, BO" sound in DOS after system post.	Change C69 value from 0.22uF to 0.47uF.	A00

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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P50	Charger	06/20/2005	Compal	Schematic issue on Charger: The RC filter should be connected on Charger LX Pin, not L-S gate Pin.	Change PR165 from 1 ohm to 0 ohm No POP PC158 200pF.	M00
2	P50	Charger	06/20/2005	Compal	Add 1 ohm_0402, 200pf RC filter to Charger LX pin as shown in attached schematic.	PR165 1 ohm_0805 PC158 200pF_0603.	X00
3	P46 P47 P48	+3.3V/+5V/+15V +1.5VRUNP /+VCCP_1P05VP +1.8VSUSP/ +0.9V_DDR_VT	06/22/2005	Compal	Voltage margining test.	Reserve PR175, PR176, PR177, PR178 and PR79 for voltage margining test.	X00
4	P44	+DCIN	07/04/2005	Dell	Under power Adapter disable.	Add PQ35, PQ26 and PR180 (No pop).	X00
5	P50	Charger	07/04/2005	Dell	Need capability for controlling the Adapter input.	Add PQ38 (No pop).	X00
6	P46	+3.3V/+5V/+15V	07/06/2005	Dell	Return to original due to SMSC EC issue already be fixed.	Add PQ39, PU16, PC171 and PR181 (No POP) Delete PR162, PC157, PU14 and PR164.	X00
7	P44 P45 P50	+DCIN Battery Conn Charger	07/06/2005	Dell	Rename pull high net from +3.3V_SRC to +3.3V_ALW.	PR1-Pin2, PR11-P IN1, Battery ESD diode, PC30-Pin1 and PR168-Pin1.	X00
8	P49	+VCC_CORE	07/06/2005	Dell	Follow Coe ref sch: change to A02.	Change PR77-Pin2 net from +PWR_SRC to +CPU_PWR_SRC Change PR87 from 150k to 147k.	X00
9	P49	+VCC_CORE	07/06/2005	Dell	Follow Coe ref sch: change to A03.	Change PR100 from 0 to 499 for Intel require Add PR182, No POP PR102 for POP option for PU5-Pin15 PG. Change net name from PGD_IN to 1.05V_RUN_PWRGD No Pop PH1 and PR88 Change RC phase node to C snubber, delete PR80, PR98 and PR118 Change PC93, PC103 and PC120 from 0.01u to 1500pF.	X00
10	P48	+1.8VSUSP/ +0.9V_DDR_VT	07/06/2005	Dell	Follow Coe ref sch: change to A02	Change net name from +0.9V_PWRGD to 0.9V_DDR_PWRGD.	X00
11	P47	+1.5VRUNP /+VCCP_1P05VP	07/06/2005	Dell	Follow Coe ref sch: change to A02 Need independent PGs and update Layout notes.	Change PG name from PGD_IN to 1.05V_RUN_PWRGD Use 1.5V PG: Add PR183 for 1.5V_RUN_PWRGD Update Layout notes.	X00
12	P48	+1.8VSUSP/ +0.9V_DDR_VT	07/13/2005	Compal	Change 0.9V input power to 1.8VSUS.	Install PJP21 for 0.9V input power.	X00
13	P46	+3.3V/+5V/+15V	07/20/2005	Dell	ILIM5 set point is too high for 6.5A OCP.	Change PR25 to 69.8K.	X00
14	P46	+3.3V/+5V/+15V	07/20/2005	Dell	ILIM3 set point is too high for 6.9A OCP.	Change PR26 to 82.5K.	X00
15	P50	Charger	07/20/2005	Dell	It is recommended to connect the ground pins of the following analog components with a separate analog ground:	PR22, PC16, PC29, PR23, PR34, PR35, PU2_pin23. Add PR184 Short this analog ground with the power ground plane at PU2_pin23.	X00
16	P48	+1.8VSUSP/ +0.9V_DDR_VT	07/20/2005	Dell	Update 1.8V output notes	Modified 1.8V: Min OCP=12.7A, not design current.	X00
17	P48	+1.8VSUSP/ +0.9V_DDR_VT	07/20/2005	Dell	PC69 need change to 0603 size.	Change PC69 to 0.1uF_25V_0603 from 0.1uF_50V_0805.	X00
18	P50	Charger	07/20/2005	Dell	Two 10uF 1210 caps are recommended for input ripple current at the 6.2A charge rate will be over 3A.	Change PC127 and PC128 to 1210 from 1206 size.	X00
19	P49	+VCC_CORE	07/20/2005	Dell	Recommend using X6S filtering capacitors for VCore decoupling Follow Team track (BITS): no: CR03709	Change PC87, PC88, PC97, PC98, PC109 and PC110 to X6S from X5R.	X00
20	P49	+VCC_CORE	07/20/2005	Dell	to match latest VCore reference schematic A03.	Depop PR104 and add PR185 resistor to jumper pin 2 to pin 38	X00

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21	P49	+VCC_CORE	07/20/2005	Dell	Change net name from H_PROCHOT# to IMVP6_PROCHOT#	Change net name from H_PROCHOT# to IMVP6_PROCHOT# on PR86 Pin2.	X00
22	P50	Charger	07/20/2005	Compal	Improve current sense accuracy	Update PR123 and PR138 Symbol Pin define for layout dimension pin define changed.	X00
23	P49	+VCC_CORE	07/20/2005	Compal	Improve Inductor DCR sense accuracy	Update PL15, PL16 and PL17 Symbol Pin define for layout dimension pin define changed.	X00
24	P50	Charger	07/21/2005	Compal	Set power limit to 130W/ 90W for ZRS.	Change PR169 to 28.7K from 200K. Add Pop Option notes. For Z/ ZUMA pop PR169: 28K, depop PR186 For R/ S pop PR186: 100K, depop PR169.	X00
25	P50	Charger	07/22/2005	Compal	Follow COE charger A02 ref. schematic.	Connected PC131 pin2 to PR165 pin2.	X00
26	P49	+VCC_CORE	08/22/2005	Compal	Cost Down:Change CPU L-S MOSFET from BSC022N03S to FDS7088SN3.	Change PQ17, PQ19 and PQ21 to FDS7088SN3.	X01
27	P49	+VCC_CORE	08/22/2005	Dell	BITS ID: CR04364. Change ISL6260 VSUM resistors to 0805 package to reduce offset error; and DROOP reisstor value	Change PR83, PR103 and PR122 to 0805 size from 0402. Chang loadline slope resistor PR119 from 9.53k to 10.5k	X01
28	P47	+1.5VRUNP /+VCCP_1P05VP	08/22/2005	Dell	Follow Coe ref sch: change to A03.	Change PL10 to 3.2UH_CDEP12D38NP_8.5A from 3.8UH_SIL104-3R8_6A. Change PR47 to 1.87K from 2.1K.	X01
29	P48	+1.8VSUSP/ +0.9V_DDR_VT	08/22/2005	Dell	Follow Coe ref sch: change to A03.	Delete PJP21 and PJP22 Jumper. VTTI only need 1.8V, no 1.5V.	X01
30	P50	Charger	08/23/2005	Dell	Follow COE charger A03 ref. schematic.	Change PR169 to 301k, PR170 to 0, PR171 to 59k, PR172 to 33.2k. Delete PR186, PC166, PC167 and PU15; depop PR166.	X01
31	P48	+1.8VSUSP/ +0.9V_DDR_VT	08/26/2005	Dell	To fix the 1.8VSUS bleed off issue at Power Down	2 of 0ohm resitors (PR186 and PR187) at PU6 pin 22 (VDD) to either 5VSUS and 5VALW.	X01
32	P46	+3.3V/+5V/+15V	08/26/2005	Compal	To fix the PC36 AL-Caps can not meet lead free reflow spec isse.	Add PC172 and change PC36 from C_25CV220AX to NIPPON, MVY25VC100MF80 due to SANYO AL Cap can not meet lead free reflow spec	X01
33	P49	+VCC_CORE	08/29/2005	Compal	To fix the PC150 AL-Caps can not meet lead free reflow spec isse.	Reserve PC173 (100U) and double footprint with PC150 (220U) Pop PC173 if needed for buzz noise, Reserve PC150 for SANYO Vendor ready AL-Caps reflow spec. and it is enough capacity (220U) to against buzz noise.	X01
34	P48	+1.8VSUSP/ +0.9V_DDR_VT	08/30/2005	Dell	BITS issue: CR20063: This is not on the reference schematic and is not asked for by Maxim.	Delete PC74.	X01
35	P49	+VCC_CORE	08/30/2005	Dell	BITS issue: CR07318: Intersil X01 ZRS Schematic Review - Vcore	Set PC100=0.015uF (decrease soft-start time) Set PR108=11.5K (set OCP=55A)	X01
36	P50	Charger	08/30/2005	Dell	BITS issue: DF20383 : Maxim ZRS X01 MAX8731 Schematic Review	Nopop PC158, set PR165=0.	X01
37	P47	+1.5VRUNP /+VCCP_1P05VP	08/31/2005	Dell	BITS issue: CR20060 : Power Good Pull Up Removed	De-populate PR183 and PR60	X01
38	P50	Charger	08/31/2005	Dell	Reserve INA194 as a Buck up.	No POP PU17, PC174, PC175 and PR188.	X01

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39	P50	Charger	09/16/2005	Dell	Update ADAPT_OC, add note.	Change PR169: 28K for R/S, 100K for Z/ZUMA Change PR171 to 121K; Change PR172 to 3.01K	X01
40	P50	Charger	09/26/2005	Compal	Change filter for derating is not enough.	1. Change PL2, PL21, PL3, PL4, PL18 and PL19 from 453215-900LMAT 1812_6A to 1812_9A; 2. Pop PL3 and PL18.	X02
41	P50	Charger	09/29/2005	Dell	Adapter OC setting update.	Pop Option notes: 1. 4@. For Zanzibar/ ZUMA pop PR169, PR172 for 90W, no pop PR189, PR190 2. 5@. For Ricker/ Suva pop PR189, PR190 for 130W, no pop PR169, PR172 3. PC160 no pop.	X02
42	P50	Charger	10/05/2005	Dell	dV/dt issue with the FBSA pin of Charger, recommend an RC filter at the pin.	Add PR191 and PC176 filter Add PR192 (No pop)	X02
43	P48	+1.8VSUSP/ +0.9V_DDR_VT	10/11/2005	Dell	Modified BST resistor to protection BOOT diode. Depop 0.9V pull high.	Change PR67 from 0 to 1. Depop PR66.	X02
44	P49	+VCC_CORE	10/14/2005	Dell	Follow Coe schematic	Change PC100 from 0.015u to 0.01uF.	X02
45	P49	+VCC_CORE	10/14/2005	Dell	Improve the temperature compensation of output voltage regulation	Change PR111 from 3.57K to 2.43K	X02
46	P49	+VCC_CORE	10/14/2005	Dell	Improve the time constant match between L/DCR and droop circuit R*C	Change PC113 from 0.01uF_NC to 0.033uF	X02
47	P49	+VCC_CORE	10/14/2005	Dell	Follow Coe schematic	PR182 Pin 1 change from H_DPRSTP# to A_GND	X02
48	P50	Charger	10/17/2005	Dell	Follow Coe schematic	Pop PR192 , No pop PR191 Connect FBSA and FBSB (pins 15 and 16) together	X02
49	P47 P46	+1.5VRUNP /+VCCP_1P05VP +3.3V/+5V/+15V	10/17/2005	Dell	Change input MLCC cap.	Pop PC145 , No pop PC47.	X02
50	P48	+VCC_CORE	10/18/2005	Dell	Change CPU L-S Layout dimension Use combination footprint	Layout dimension from FDS7088SN3_S08 to FDS7088SN3_S08_3P	X02
51	P46 P48	+3.3V/+5V/+15V +1.8VSUSP/ +0.9V_DDR_VT	10/25/2005	Dell	Update 3V, 5V and 1.8V OC to meet power Budgets	Change PR76 from 48.7k to 36.5k Change PR26 from 82.5k to 71.5k Change PR25 from 69.8k to 19.1k	X02
52	P50	Charger	10/26/2005	Compal	Add 1 ohm, 200pf RC filter to Charger LX pin same as Travis.	Change PR165 from 0 to 1, Pop PC158 220pF.	X02
53	P50	Charger	10/27/2005	Dell	Adapter OC UL circuit update	1. change PR169 from 4@301k to 4@49.9k 2. change PR172 from 4@71.5k to 4@9.31k 3. change PR171 from 68.1k to 13.3k 4. change PR189 from 5@215k to 5@33.2k 5. change PR190 from 5@121k to 5@15k 6. change PR166 from @499k to 976k	X02
54	P47	+1.8VSUSP/ +0.9V_DDR_VT	11/11/2005	Dell	Follow Coe A05 schematic	Delete PR68 0 ohms on pin7 driven by RUN_ON.	A00
55	P49	Charger	11/11/2005	Dell	Change Charger input caps size due to material EOL.	Change PC127 and PC128 from 1210 to 1206.	A00

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